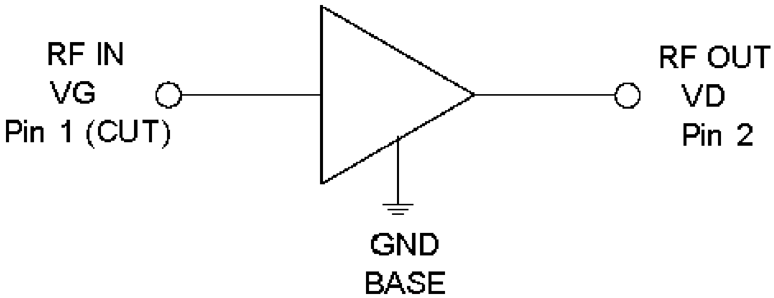
RFHA1027

500W GaN Wide-Band Pulsed Power Amplifier

Package: Flanged Ceramic, 2 pin

The RFHA1027 is a 50V 500W high power discrete amplifier designed for L-Band pulsed radar, air traffic control and surveillance and general purpose broadband amplifiers applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, these high performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RFHA1027 is a matched power transistor packaged in a hermetic, flanged ceramic package. The package provides excellent thermal stability through the use of advanced heat-sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of single, optimized matching networks that provide wideband gain and power performance in a single amplifier.



Functional Block Diagram

Features

- Wideband Operation: 1.2GHz to1.4GHz
- Advanced GaN HEMT Technology
- Advanced Heat-Sink Technology
- Optimized Evaluation Board Layout for 50Ω Operation
- Integrated Matching Components for High Terminal Impedances
- 50V Operation Typical Performance
  - Output Pulsed Power 500W
  - Pulse Width 1ms, Duty Cycle 10%
  - Small Signal Gain 16dB
  - High Efficiency 55%
  - -40°C to 85°C Operation Temperature

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers

Ordering Information

RFHA1027S2	Sample bag with 2 pieces
RFHA1027SB	Bag with 5 pieces
RFHA1027SQ	Bag with 25 pieces
RFHA1027SR	7” short reel with 50 pieces
RFHA1027TR13	13” reel with 250 pieces
RFHA1027PCBA-410	Fully Assembled Evaluation Board Optimized for 1.2GHz to1.4GHz; 50V

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.
DS140204

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to 2	V
Operating Voltage	65	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_C)	-40 to +85	°C
Operating Junction Temperature (T_J)	200	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)*	1.8E + 07	Hours
MTTF (T_J < 250°C, 95% Confidence Limits)*	1.1E + 05	Hours
Thermal Resistance, R_{TH} (Junction to Case)		°C/W
T_C = 85°C, DC Bias Only	0.90	
T_C = 85°C, 100µs Pulse, 10% Duty Cycle	0.13	
T_C = 85°C, 1ms Pulse, 10% Duty Cycle	0.25	

* MTTF – median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.

Caution! ESD sensitive device.

RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2011/65/EU.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J – T_C) / R_{TH\ J-C}$ and $T_C = T_{CASE}$

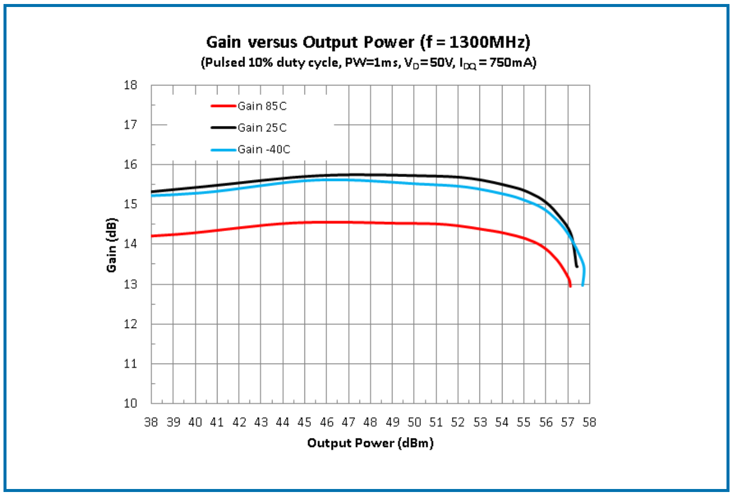
Nominal Operating Parameters

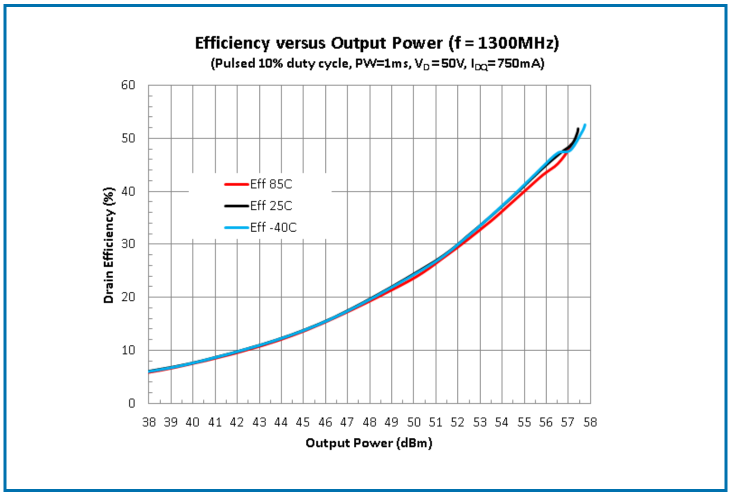
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		50		V	
Gate Voltage (V_{GSQ})	-8	-3.3	-2	V	
Drain Bias Current		750		mA	
Frequency of Operation	1200		1400	MHz	
DC Functional Test					
$I_{G(OFF)}$ – Gate Leakage			3	mA	V_G = -8V, V_D = 0V
$I_{D(OFF)}$ – Drain Leakage			15	mA	V_G = -8V, V_D = 50V
$V_{GS(TH)}$ – Threshold Voltage		-3.5		V	V_D = 50V, I_D = 40mA
$V_{DS(ON)}$ – Drain Voltage at high current		0.43		V	V_G = 0V, I_D = 1.5A

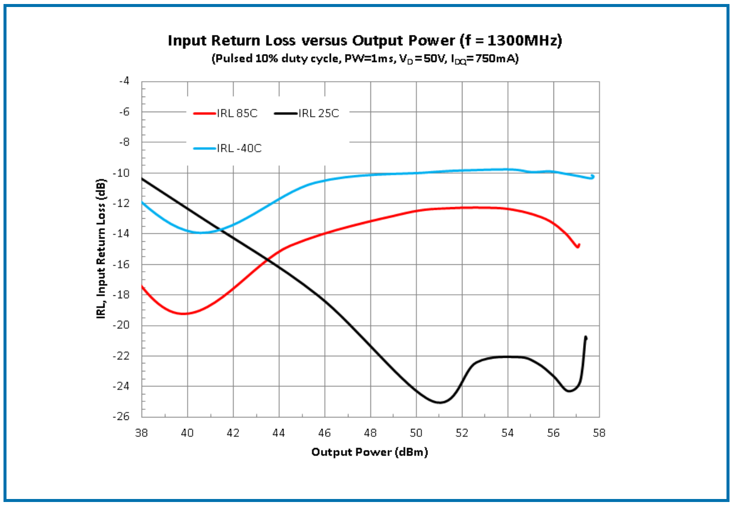
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Functional Test					**Test Conditions: PW = 1ms, DC = 10%, V_{DSQ} = 50V, I_{DQ} = 750mA, T = 25ºC, Performance in a standard tuned test fixture.**
Power Gain	12.5	13.6		dB	f = 1200MHz, P_{IN} = 44dBm
Input Return Loss			-5	dB	
Output Power	56.5	57.6		dBm	
Drain Efficiency		53		%	
Power Gain	12.5	13.3		dB	f = 1300MHz, P_{IN} = 44dBm
Input Return Loss			-5	dB	
Output Power	56.5	57.3		dBm	
Drain Efficiency		55		%	
Power Gain	12.5	12.8		dB	f = 1400MHz, P_{IN} = 44dBm
Input Return Loss			-5	dB	
Output Power	56.5	56.8		dBm	
Drain Efficiency		54		%	
RF Typical Performance					
Frequency Range	1200		1400	MHz	
Low Power Gain		15.8		dB	P_{OUT} = 36dBm [1,2]
Power Gain		13.3		dB	P_{IN} = 44dBm [1,2]
Gain Variation with Temperature			-0.019	dB/°C	At peak output power [1,2]
Output Power (P_{SAT})		57		dBm	Peak output power [1,2]
		500		W	
Drain Efficiency		54		%	At peak output power [1,2]

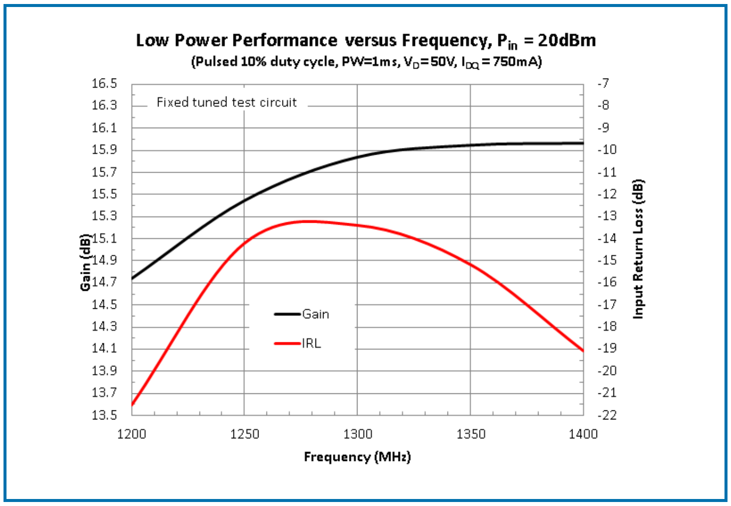
[1] Test Conditions: PW = 1ms, DC = 10%, V_{DSQ} = 50V, I_{DQ} = 750mA, T = 25ºC.
[2] Performance in a standard tuned test fixture.

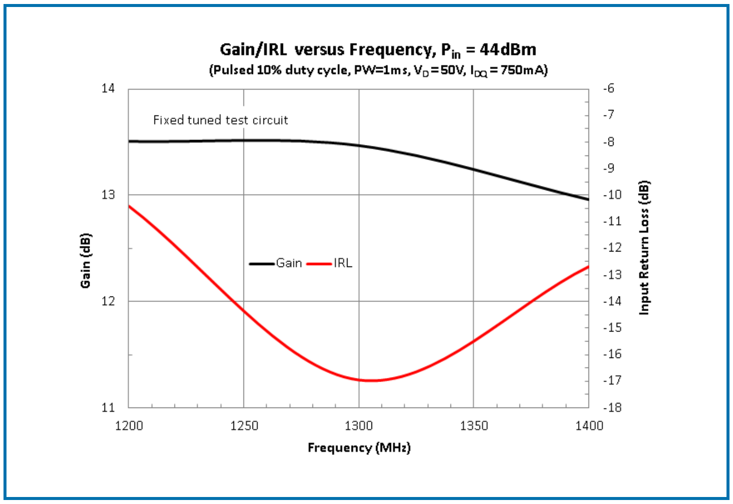
Typical Performance in Standard Fixed Tuned Test Fixture: T = 25°C unless noted

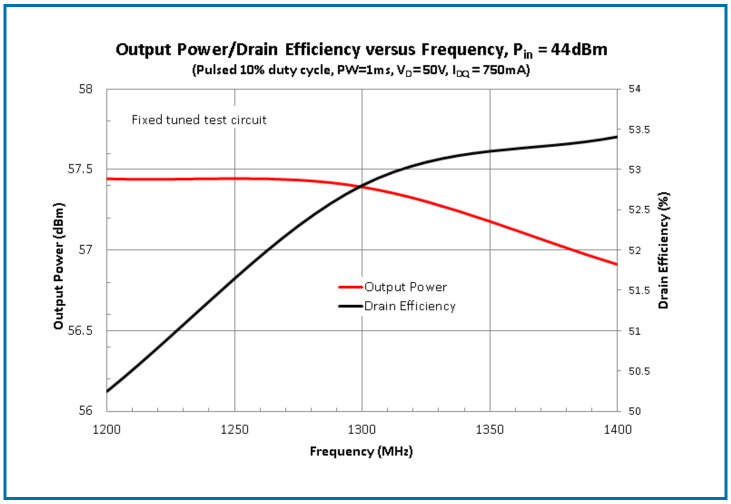




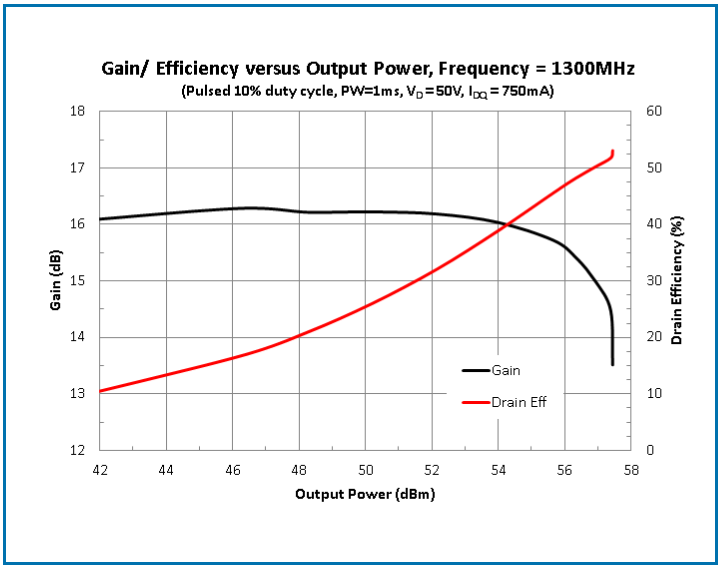


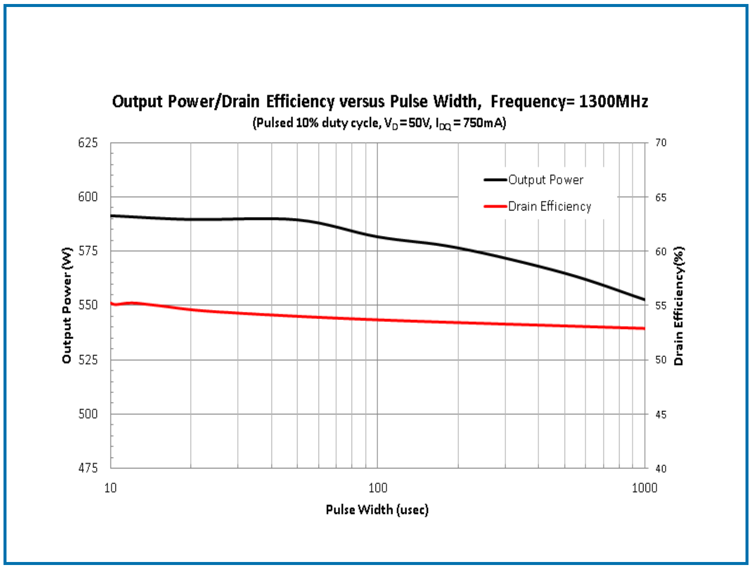


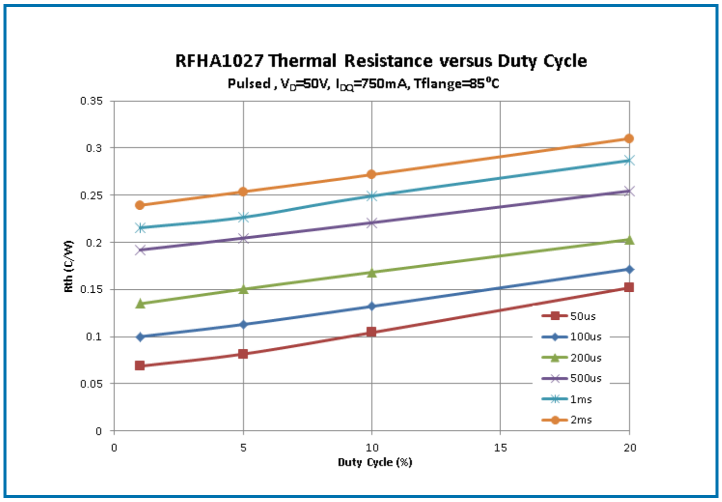


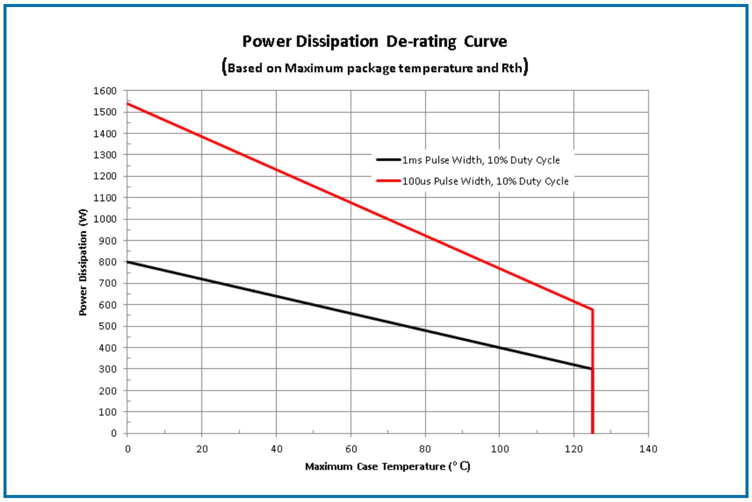


Typical Performance in Standard Fixed Tuned Test Fixture: T = 25°C unless noted (continued)

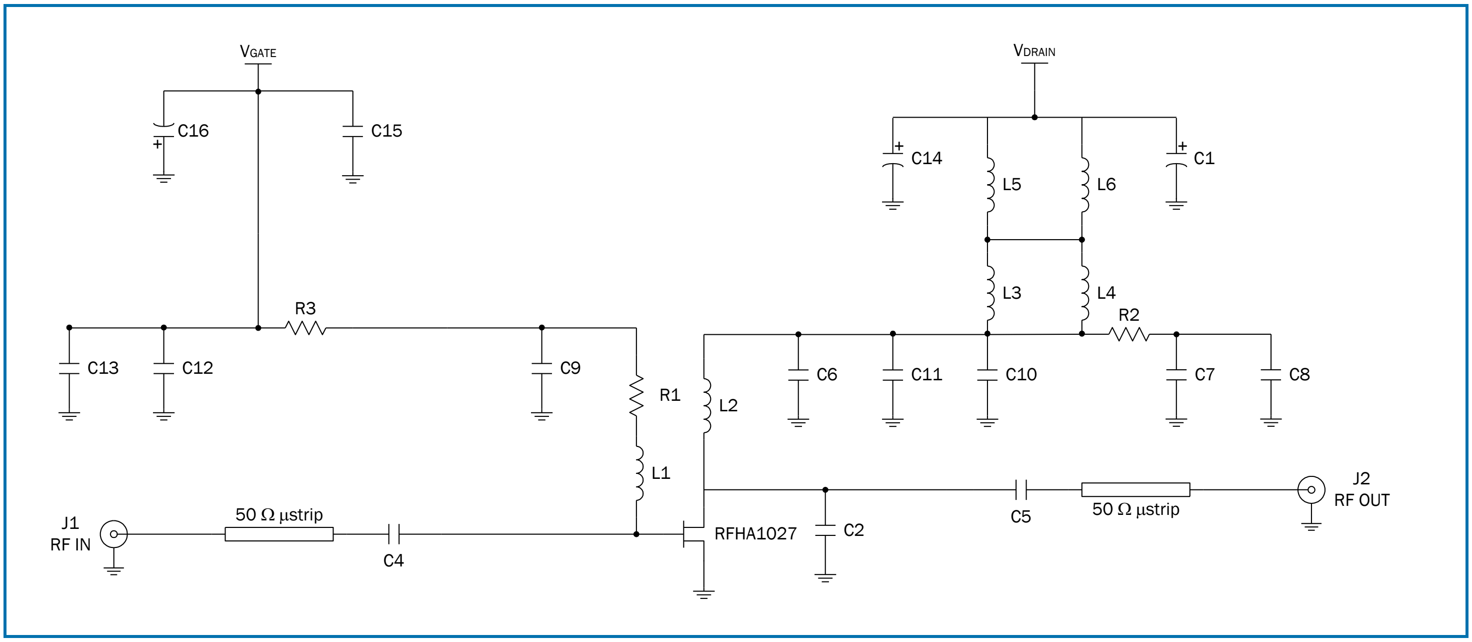








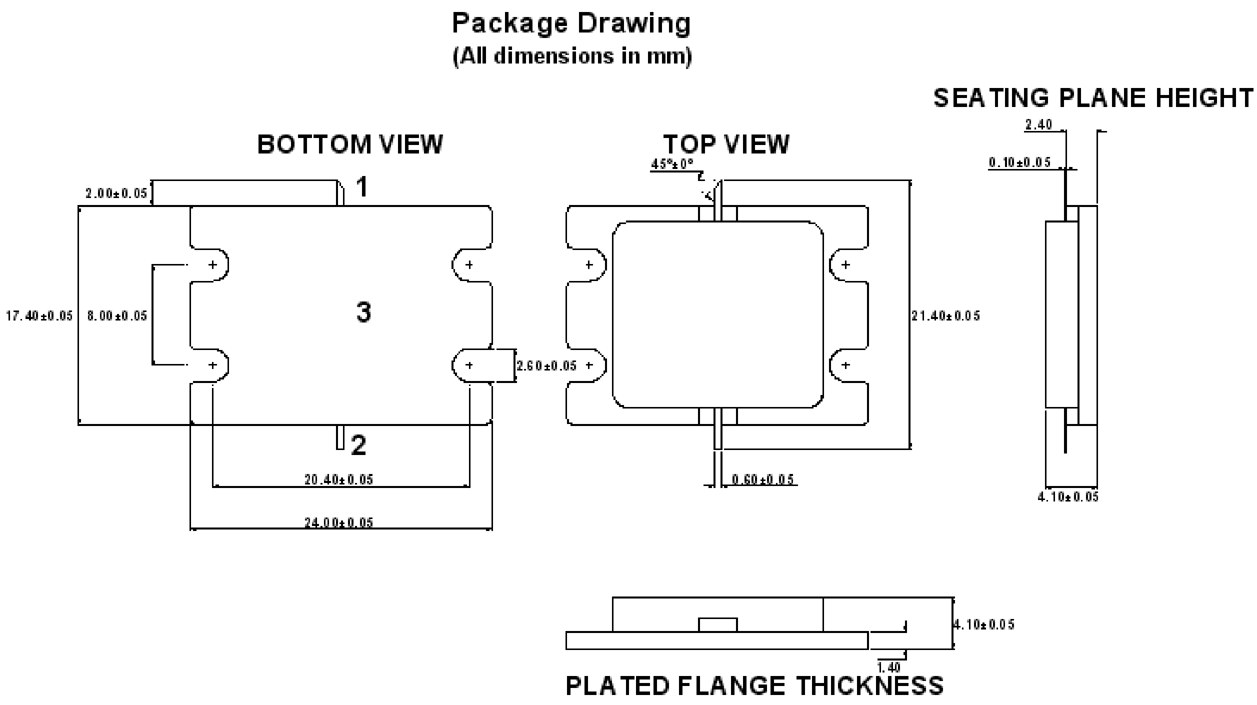
Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

Component	Value	Manufacturer	Part Number
C1	680uF	Panasonic	EEU-FC2A681
C11	0.1uF	Murata	GRM32NR72A104KA01L
C13	0.1uF	Panasonic	ECJ-2YB1H104K
C14,C16	10uF	Panasonic	ECA-2AM100
C2	2.7pF	ATC	ATC800A2R7BT
C4, C6, C9, C10	100pF	ATC	ATC800A101JT
C5	150pF	ATC	ATC800B151JT300X
C7, C12	10000pF	Panasonic	ECJ-2VB2A103K
C8	0.1uF	Panasonic	ECJ-2VB2A104K
L1	68nH	Coilcraft	1812SMS-68NJLB
L2	82nH	Coilcraft	1812SMS-82NJLB
L3, L4	75 ohm, 10A	Steward	35F0121-1SR-10
L5, L6	115 ohm, 10A	Steward	28F0181-1SR-10
R1, R3	10 ohms	Panasonic	ERJ-8GEYJ100V
R2	51 ohms	Panasonic	ERJ-8GEYJ510

Package Drawing (Dimensions in millimeters)



Pin Names and Descriptions

Pin	Name	Description
1	GATE	V_G RF Input
2	DRAIN	V_D RF Output
3	SOURCE	Ground Base

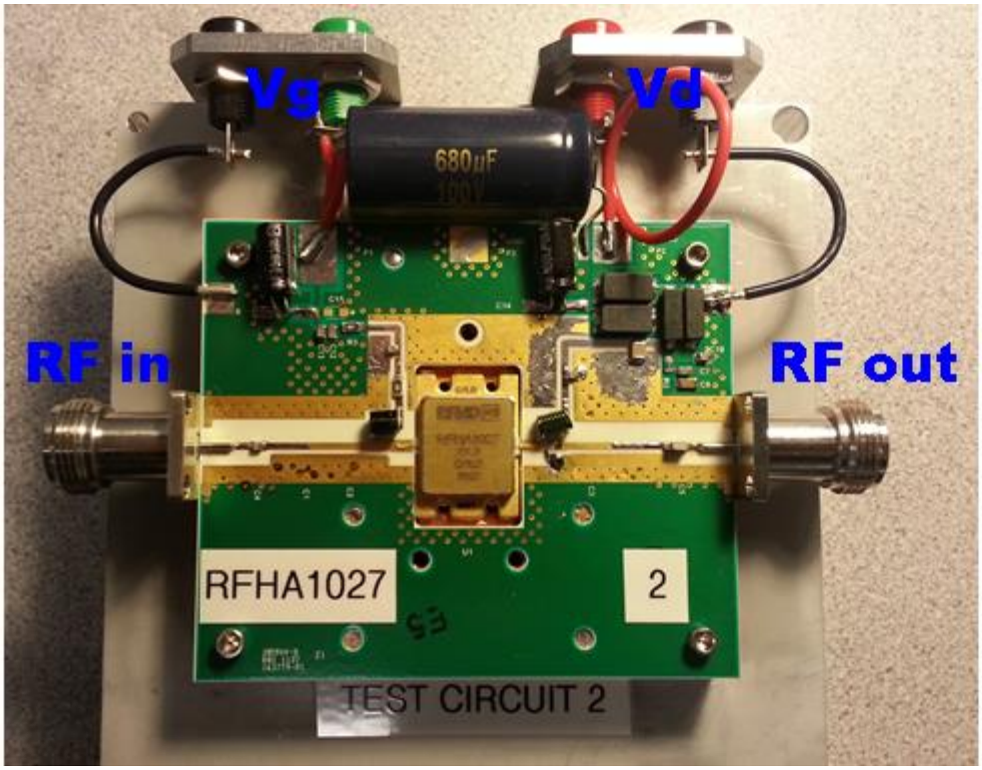
Bias Instruction for RFHA1027 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering evaluation board.

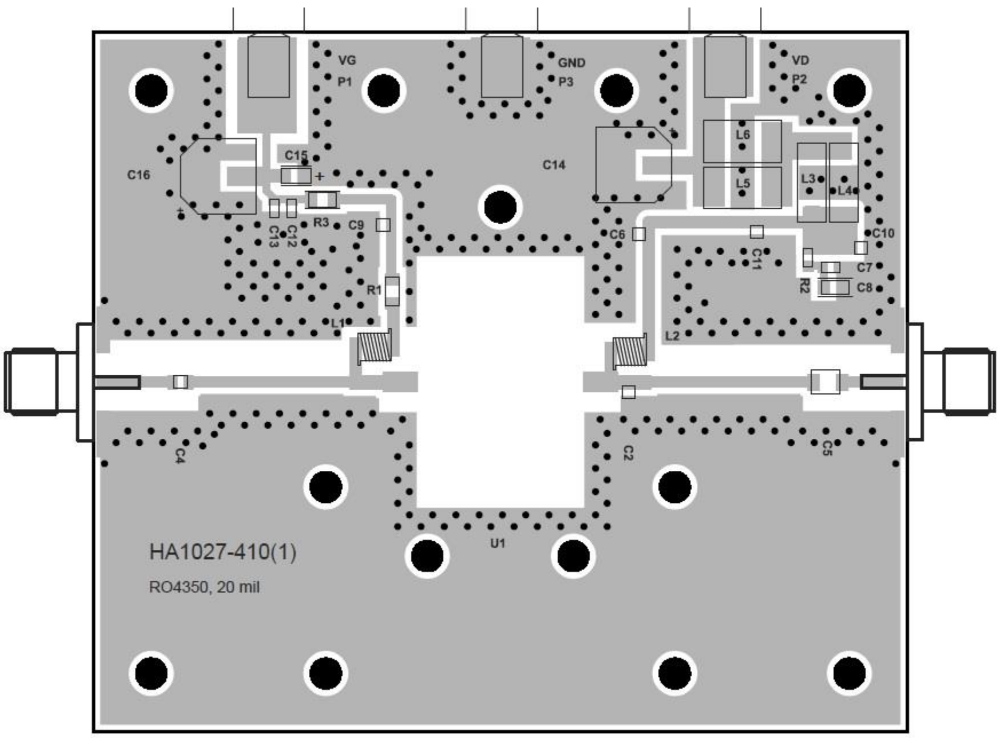
1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -8V to VG.
4. Apply 50V to VD.
5. Increase V_G until drain current reaches 750mA or desired bias point.
6. Turn on the RF input.

IMPORTANT NOTE: Depletion mode device - when biasing the device V_G must be applied BEFORE V_D. When removing bias V_D must be removed BEFORE V_G is removed. Failure to follow sequencing will cause the device to fail.

Note: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board.

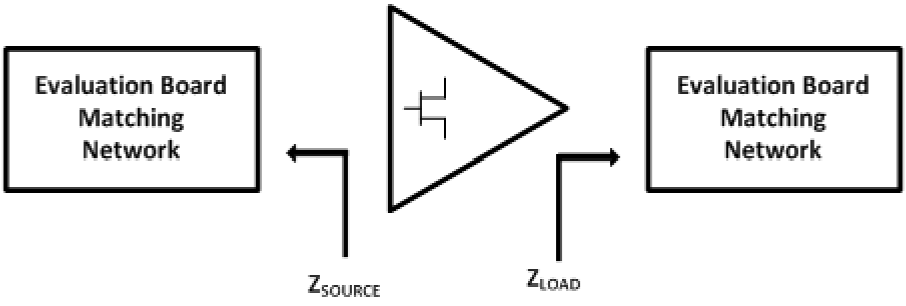


Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
1200	38.1 + j4.5	18 – j1.0
1300	37.6 + j4.6	16 + j0.5
1400	36.7 + j4.5	17 + j1.6



Device Handling/Environmental Conditions

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.