

Vishay Siliconix

N-Channel 1.2-V (G-S) MOSFET

Marking Code

XXX

Part # code

PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)	
	0.026 at V _{GS} = 4.5 V	9 ^a		
8	0.030 at V_{GS} = 2.5 V	9 ^a		
	0.037 at V _{GS} = 1.8 V	9 ^a	8.6 nC	
	0.052 at V _{GS} = 1.5 V	9 ^a		
	0.089 at V _{GS} = 1.2 V	9 ^a		

1.60 mm

PowerPAK SC-75-6L-Single

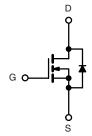
1.60 mm

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-75 Package
 - Small Footprint Area
 - Low On-Resistance

APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable
 Devices
- DC/DC Converter



Ordering Information: SiB414DK-T1-GE3 (Lead (Pb)-free and Halogen-free)

Lot Traceability and Date code

N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	8	V	
Gate-Source Voltage		V _{GS}	± 5		
	T _C = 25 °C		9 ^a		
Continuous Drain Current ($T_1 = 150 \ ^{\circ}C$)	T _C = 70 °C	I _D	9 ^a	A	
	T _A = 25 °C	U	7.9 ^{b, c}		
	T _A = 70 °C		6.3 ^{b, c}		
Pulsed Drain Current		I _{DM}	20		
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	9 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	'5	2 ^{b, c}		
	T _C = 25 °C		13		
Maximum Power Dissipation	T _C = 70 °C	PD	8.4	w	
	T _A = 25 °C	U	2.4 ^{b, c}		
	T _A = 70 °C		1.6 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	<u></u>		
Soldering Recommendations (Peak Temperature	-	260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	41	51	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	7.5	9.5	0/11

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 105 °C/W.

d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.



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SPECIFICATIONS $T_J = 25 \ ^{\circ}C$, unless oth	erwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static						•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	8			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μΑ		9.42		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η - 200 μΑ		- 2.52			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	0.35		1	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 5 V$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 8 V, V_{GS} = 0 V$			1	μΑ	
		$V_{DS} = 8 V, V_{GS} = 0 V, T_{J} = 55 \ ^{\circ}C$			10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS}{\leq}5$ V, $V_{GS}{=}4.5$ V	20			А	
Drain-Source On-State Resistance ^a		$V_{GS} = 4.5 \text{ V}, I_D = 7.9 \text{ A}$		0.021	0.026	Ω	
		V _{GS} = 2.5 V, I _D = 7.4 A		0.0246	0.030		
	R _{DS(on)}	$V_{GS} = 1.8 \text{ V}, I_{D} = 6.6 \text{ A}$		0.030	0.037		
		V _{GS} = 1.5 V, I _D = 1.92 A		0.037	0.052		
		V _{GS} = 1.2 V, I _D = 1.02 A		0.059	0.089		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 4 V, I _D = 7.9 A		27		S	
Dynamic ^b							
Input Capacitance	C _{iss}			732		pF	
Output Capacitance	C _{oss}	V_{DS} = 4 V, V_{GS} = 0 V, f = 1 MHz		280			
Reverse Transfer Capacitance	C _{rss}			195			
Tatal Cata Charge		$V_{DS} = 4 V, V_{GS} = 5 V, I_{D} = 7.9 A$		9.35	14.03	nC	
Total Gate Charge	Qg			8.6	13		
Gate-Source Charge	Q _{gs}	V_{DS} = 4 V, V_{GS} = 4.5 V, I_{D} = 7.9 A		0.53			
Gate-Drain Charge	Q _{gd}			2.78			
Gate Resistance	Rg	f = 1 MHz		3.6		Ω	
Turn-On Delay Time	t _{d(on)}			7	10.5		
Rise Time	t _r	V_{DD} = 4 V, R_L = 0.64 Ω		13	19.5	- ns	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_{\text{D}}\cong$ 6.3 A, V_{GEN} = 4.5 V, R_{g} = 1 Ω		50	75		
Fall Time	t _f			14	21		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	ا _S	T _C = 25 °C			9	•	
Pulse Diode Forward Current	I _{SM}			ſ	20	A	
Body Diode Voltage	V _{SD}	$I_{S} = 3.2 \text{ A}, V_{GS} = 0 \text{ V}$		0.7	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			23	35	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			8.1	12.15	nC	
Reverse Recovery Fall Time	t _a	$I_F = 3.2 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^\circ\text{C}$		13.3		ns	
Reverse Recovery Rise Time	t _b			9.6			

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

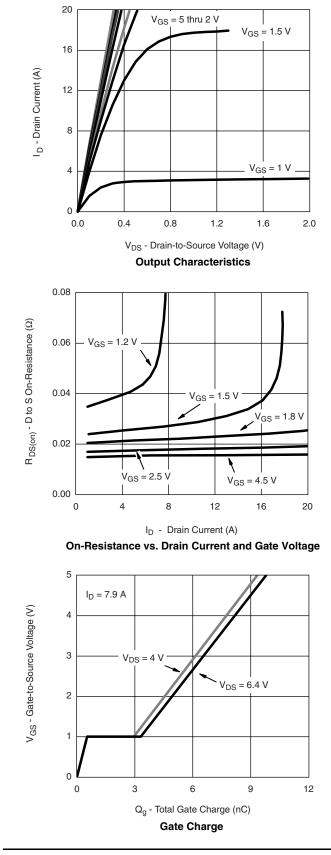
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

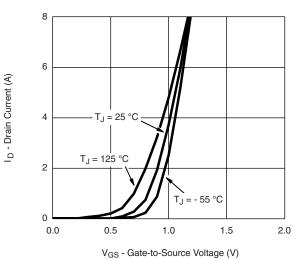




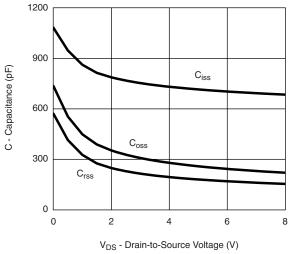
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

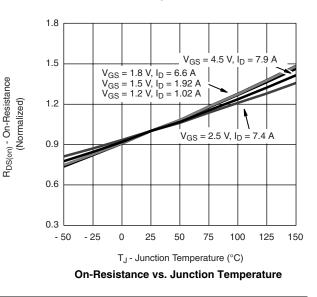




Transfer Characteristics





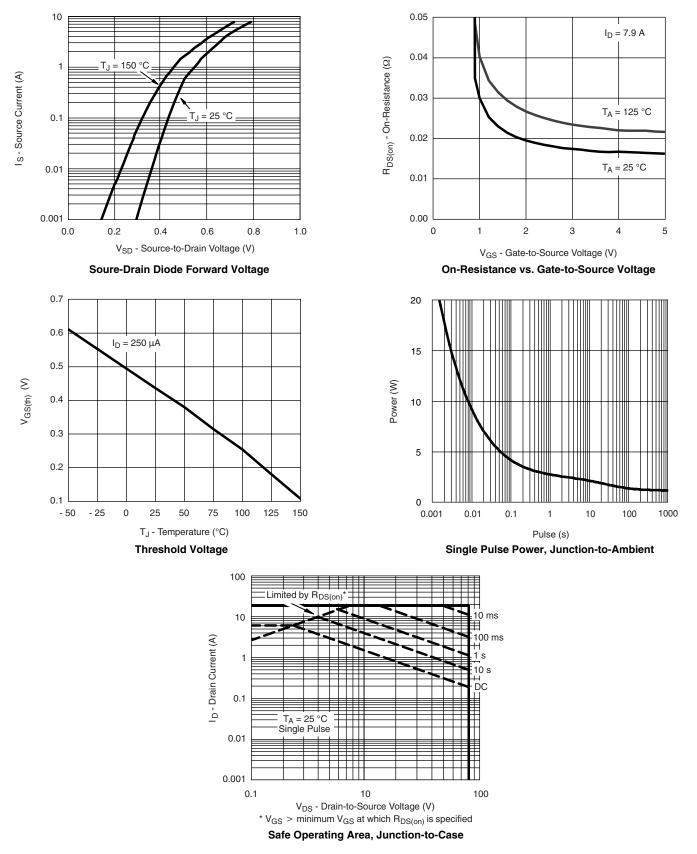


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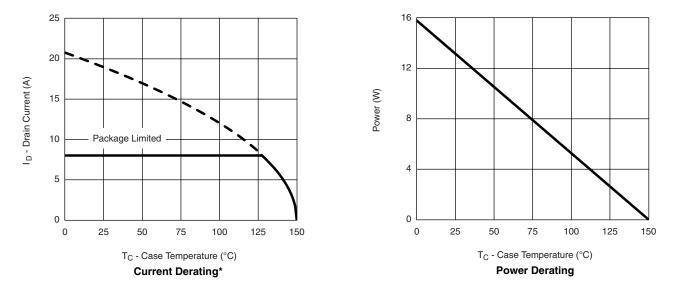






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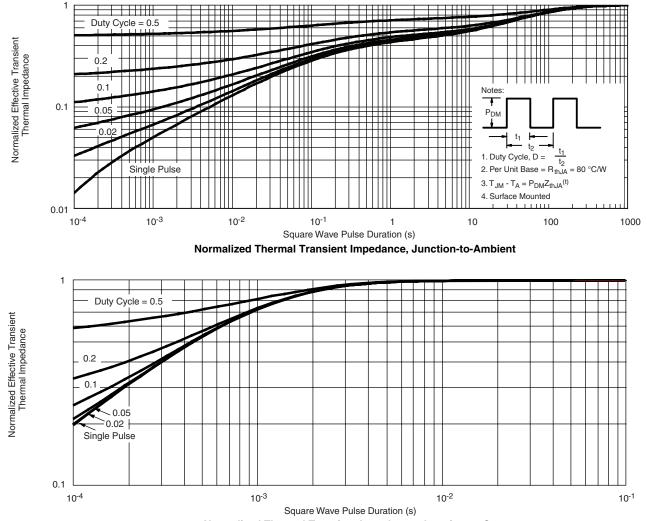


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?74635.



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