Freescale Semiconductor
Technical Data

Document Number: MRF7S19100N
Rev. 3, 12/2008

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio and WLL applications.

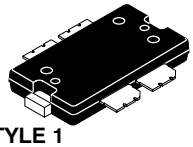
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1000 mA, P_{out} = 29 Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 17.5 dB
  Drain Efficiency — 30%
  Device Output Signal PAR — 6.1 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — -38 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 1960 MHz, 100 Watts CW Peak Tuned Output Power
- P_{out} @ 1 dB Compression Point ≥ 100 W CW

Features

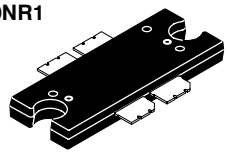
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Designed for Digital Predistortion Error Correction Systems
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF7S19100NR1
MRF7S19100NBR1

1930-1990 MHz, 29 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF7S19100NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF7S19100NBR1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +200	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 82°C, 100 W CW Case Temperature 79°C, 29 W CW	$R_{\theta JC}$	 0.57 0.68	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

freescale semiconductor

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	500	nAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 320 μAdc)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 1000 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.2 Adc)	$V_{DS(on)}$	0.2	0.24	0.4	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.54	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	553.5	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, P_{out} = 29 W Avg., f1 = 1930 MHz, f2 = 1990 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

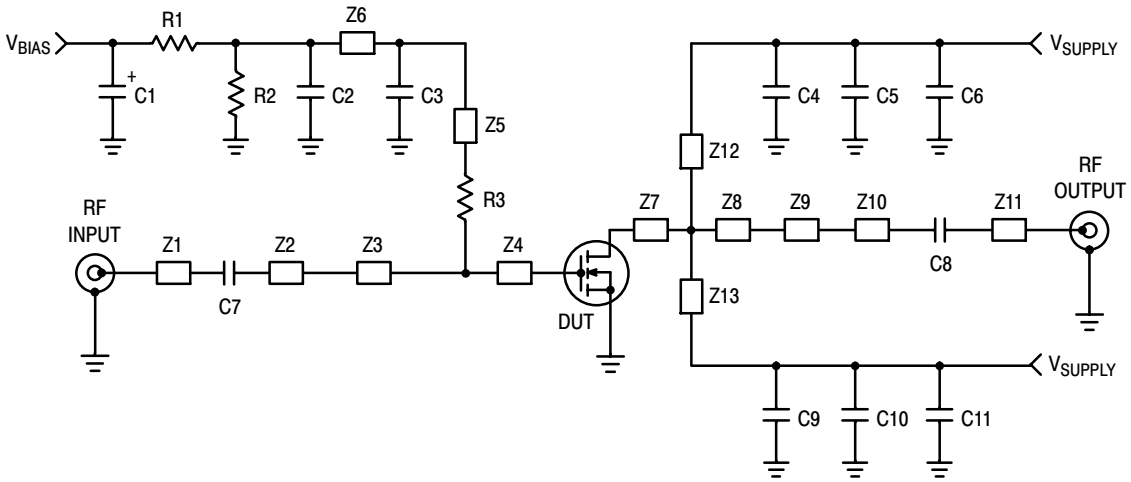
Power Gain	G_{ps}	16.5	17.5	19.5	dB
Drain Efficiency	η_D	28.5	30	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-38	-36	dBc
Input Return Loss	IRL	—	-12	-10	dB

1. V_{GG} = 11/10 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, 1930 - 1990 MHz Bandwidth					
Video Bandwidth @ 100 W PEP P_{out} where IM3 = -30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	30	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 29 W Avg.	G_F	—	1	—	dB
Average Group Delay @ P_{out} = 100 W CW, f = 1960 MHz	Delay	—	2.15	—	ns
Part - to - Part Insertion Phase Variation @ P_{out} = 100 W CW, f = 1960 MHz, Six Sigma Window	ΔΦ	—	28.8	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.019	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.015	—	dBm/°C



Z1	0.744″ x 0.084″ Microstrip	Z8	0.319″ x 0.880″ Microstrip
Z2	0.383″ x 0.084″ Microstrip	Z9	0.390″ x 0.215″ Microstrip
Z3	0.600″ x 0.230″ Microstrip	Z10	0.627″ x 0.084″ Microstrip
Z4	0.505″ x 0.800″ Microstrip	Z11	0.743″ x 0.084″ Microstrip
Z5	1.086″ x 0.080″ Microstrip	Z12, Z13	1.326″ x 0.121″ Microstrip
Z6	0.452″ x 0.080″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030, ε_r = 2.55
Z7	0.161″ x 0.880″ Microstrip		

Figure 1. MRF7S19100NR1(NBR1) Test Circuit Schematic

Table 6. MRF7S19100NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	10 μF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C2, C5, C6, C10, C11	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C3, C7	5.1 pF Chip Capacitors	ATC100B5R1BT500XT	ATC
C4, C9	8.2 pF Chip Capacitors	ATC100B8R2BT500XT	ATC
C8	10 pF Chip Capacitor	ATC100B100BT500XT	ATC
R1	1 KΩ, 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	10 KΩ, 1/4 W Chip Resistor	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

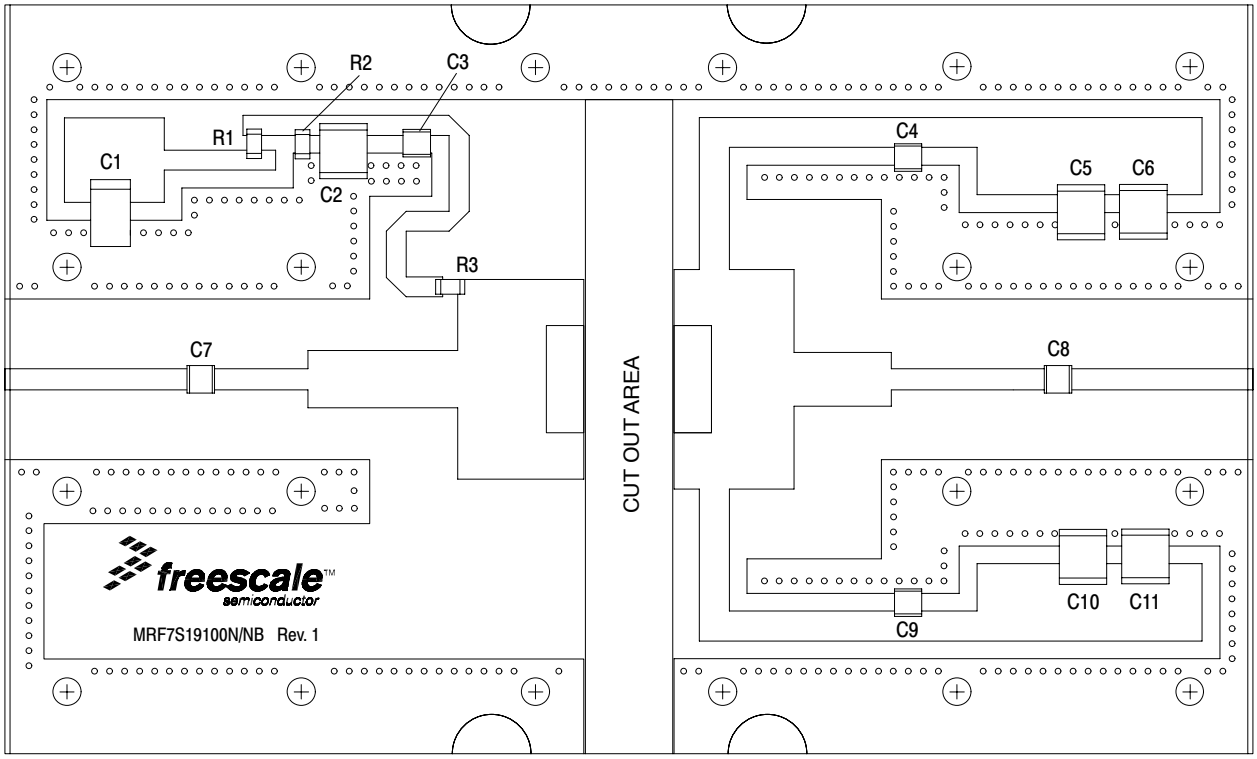


Figure 2. MRF7S19100NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

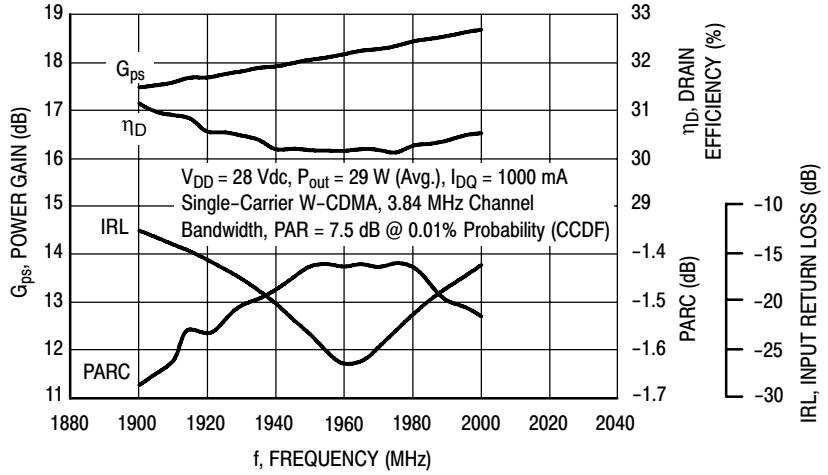


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 29 Watts Avg.

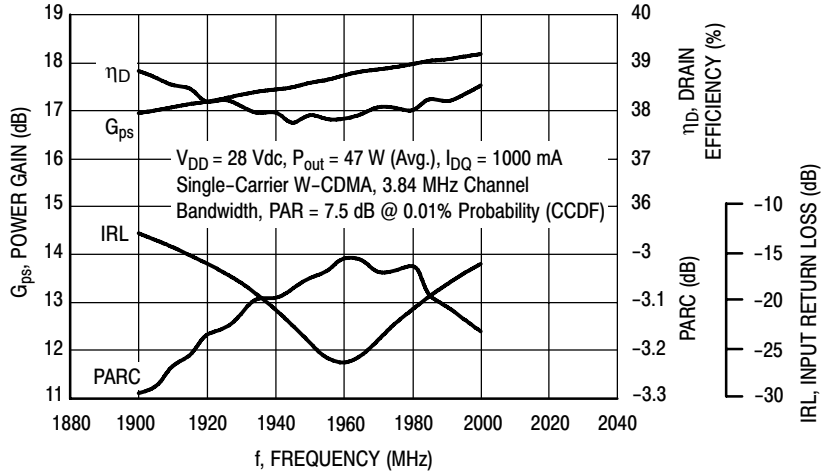


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 47 Watts Avg.

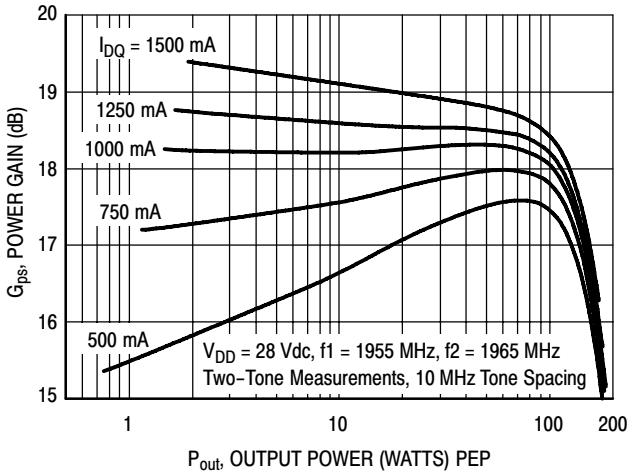


Figure 5. Two-Tone Power Gain versus Output Power

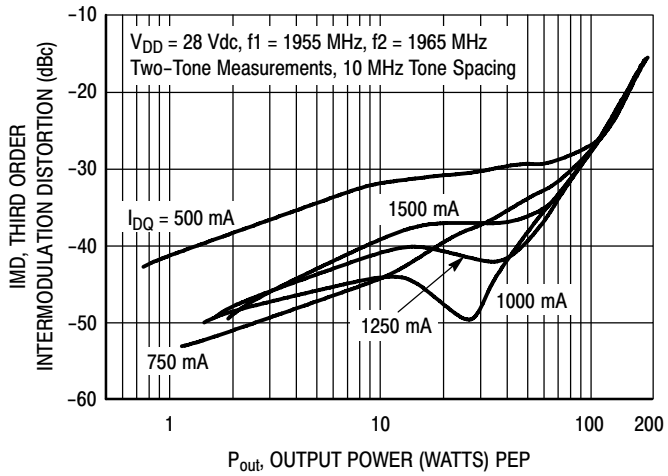


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

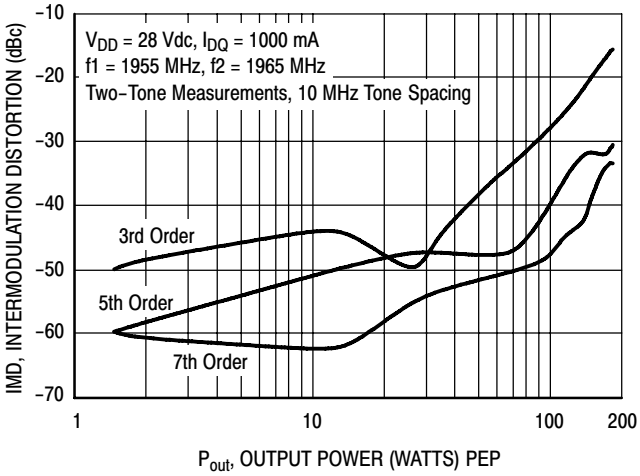


Figure 7. Intermodulation Distortion Products versus Output Power

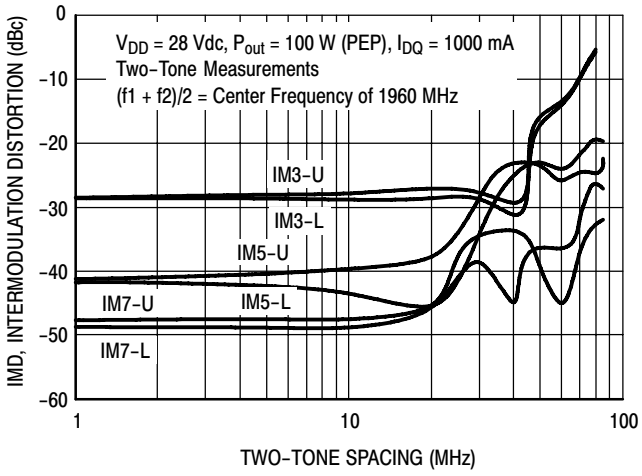


Figure 8. Intermodulation Distortion Products versus Tone Spacing

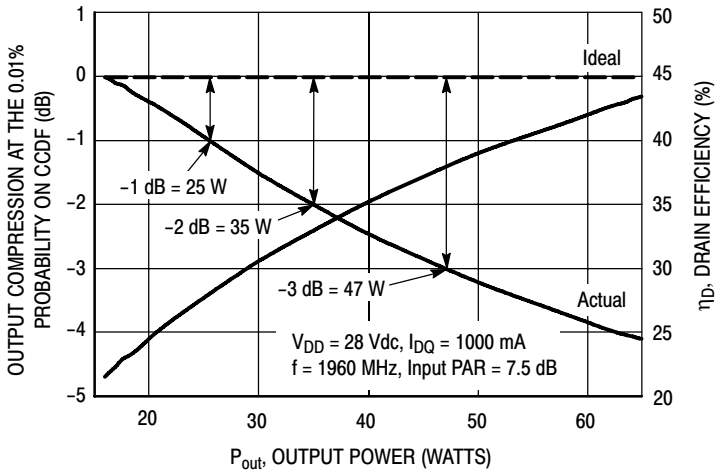


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

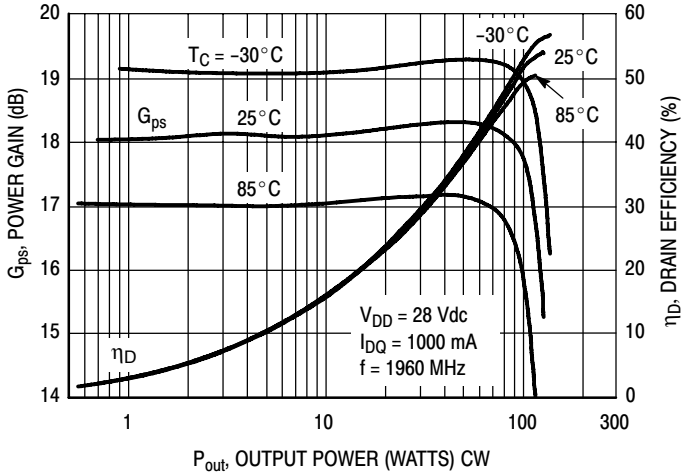


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

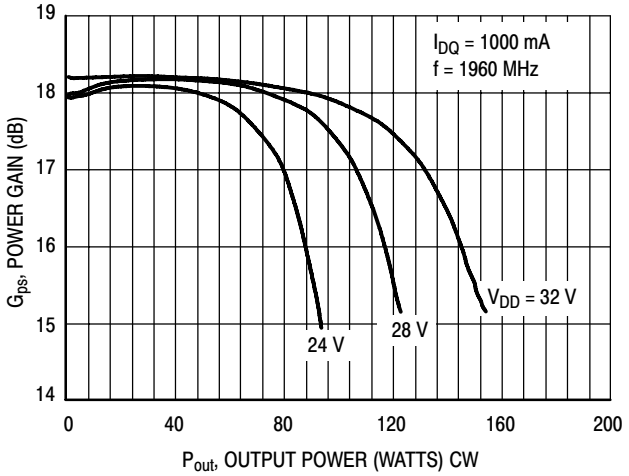
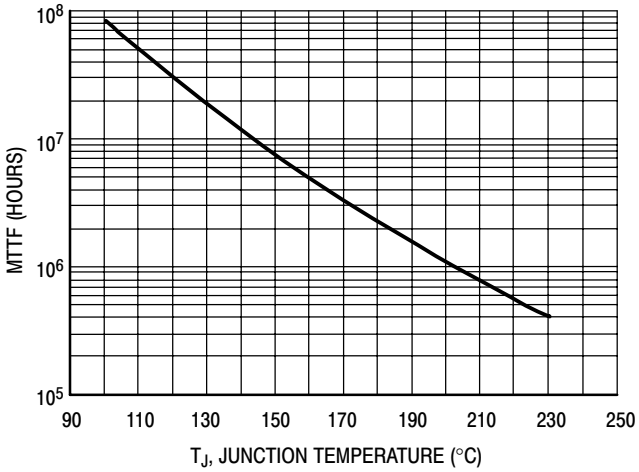


Figure 11. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 29 W Avg., and η_D = 30%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 12. MTTF Factor versus Junction Temperature

W-CDMA TEST SIGNAL

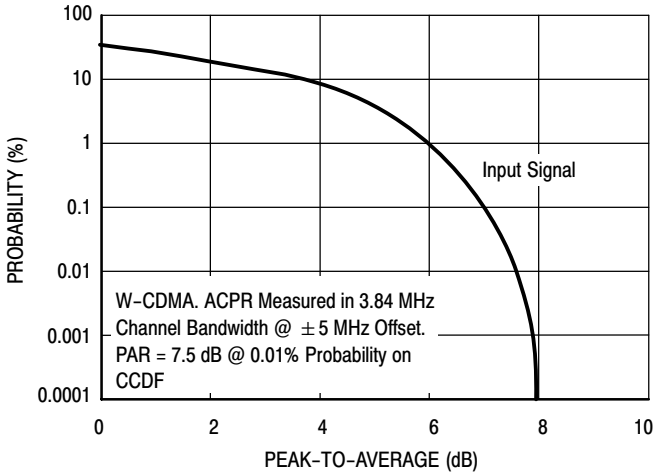


Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

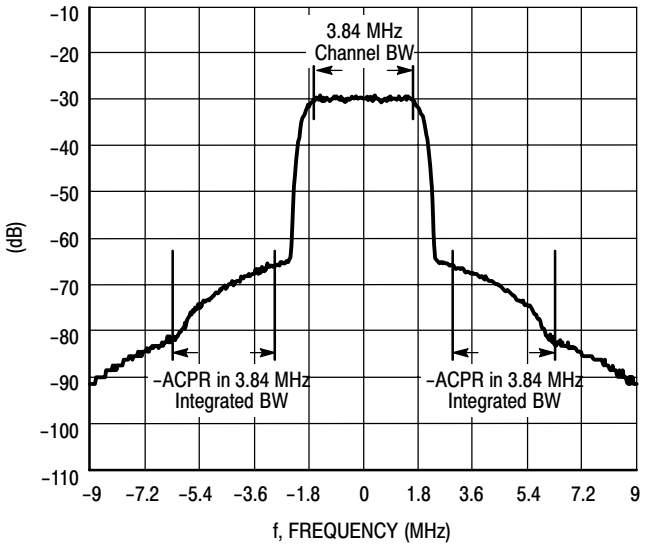
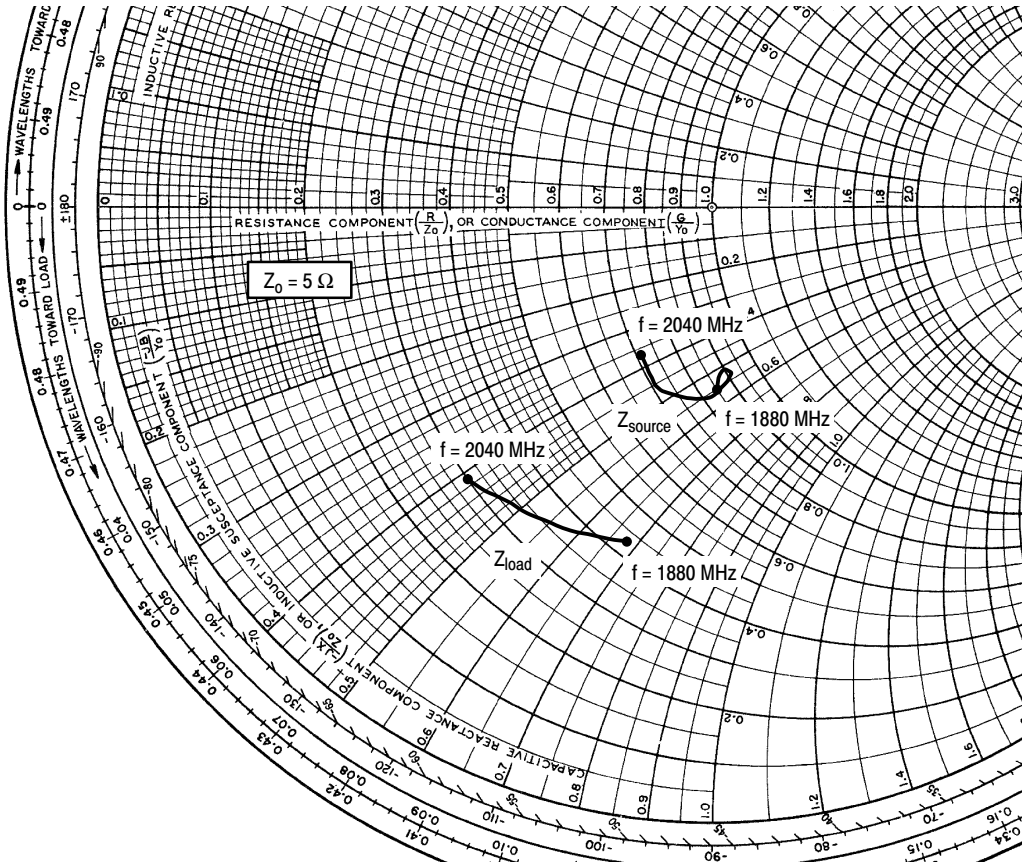


Figure 14. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, P_{out} = 29 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1880	4.257 - j2.758	2.143 - j3.408
1900	4.388 - j2.617	2.038 - j3.236
1920	4.521 - j2.560	1.944 - j3.066
1940	4.568 - j2.630	1.858 - j2.898
1960	4.424 - j2.758	1.775 - j2.725
1980	4.124 - j2.800	1.708 - j2.550
2000	3.819 - j2.611	1.643 - j2.387
2020	3.567 - j2.292	1.572 - j2.223
2040	3.525 - j1.844	1.487 - j2.029

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

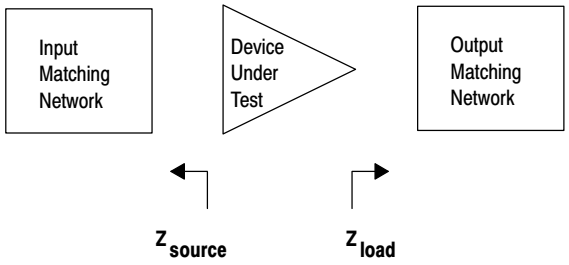
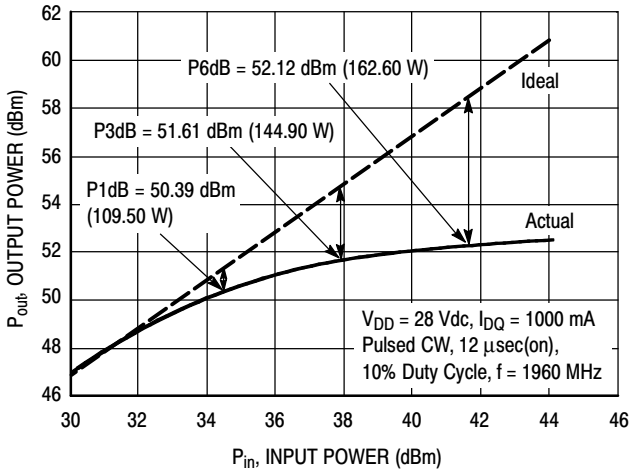


Figure 15. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

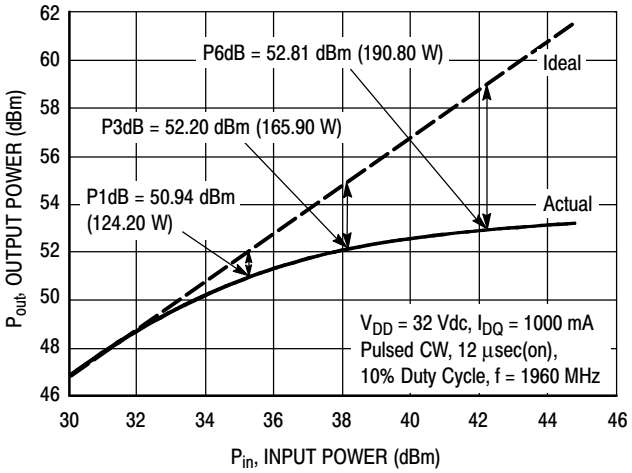


NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	4.39 - j5.66	1.81 - j3.27

Figure 16. Pulsed CW Output Power versus Input Power



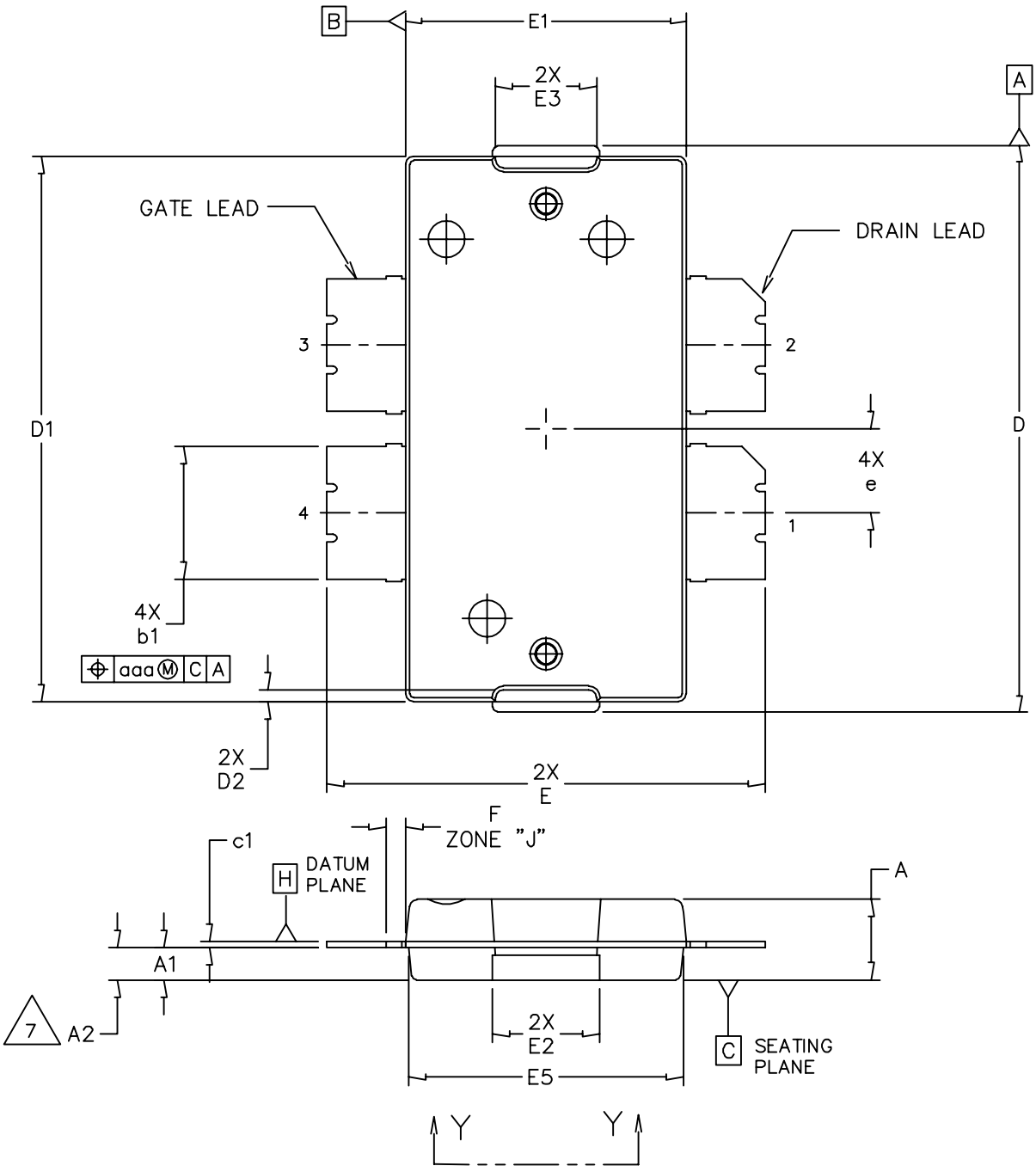
NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	4.39 - j5.66	1.81 - j3.27

Figure 17. Pulsed CW Output Power versus Input Power

PACKAGE DIMENSIONS



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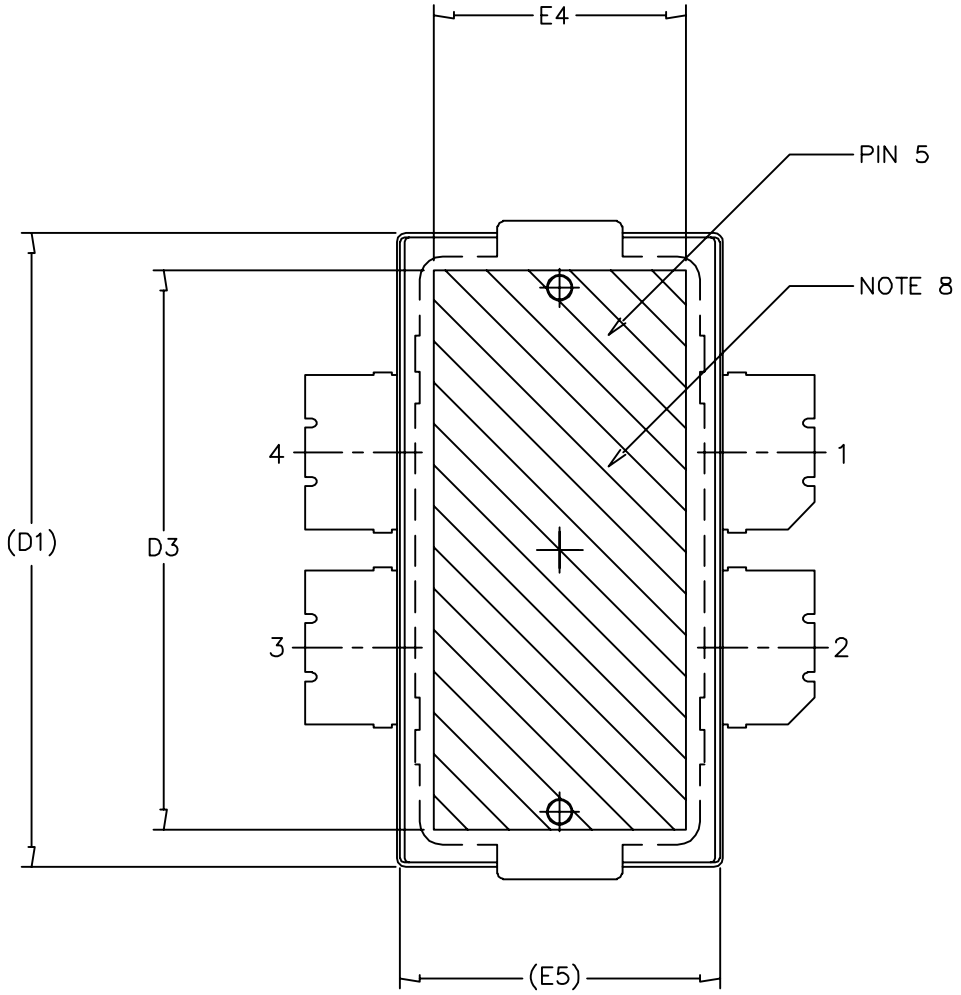
	CASE NUMBER: 1486−03	13 AUG 2007
	STANDARD: NON−JEDEC	



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TITLE: TO−270 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D
	CASE NUMBER: 1486−03	13 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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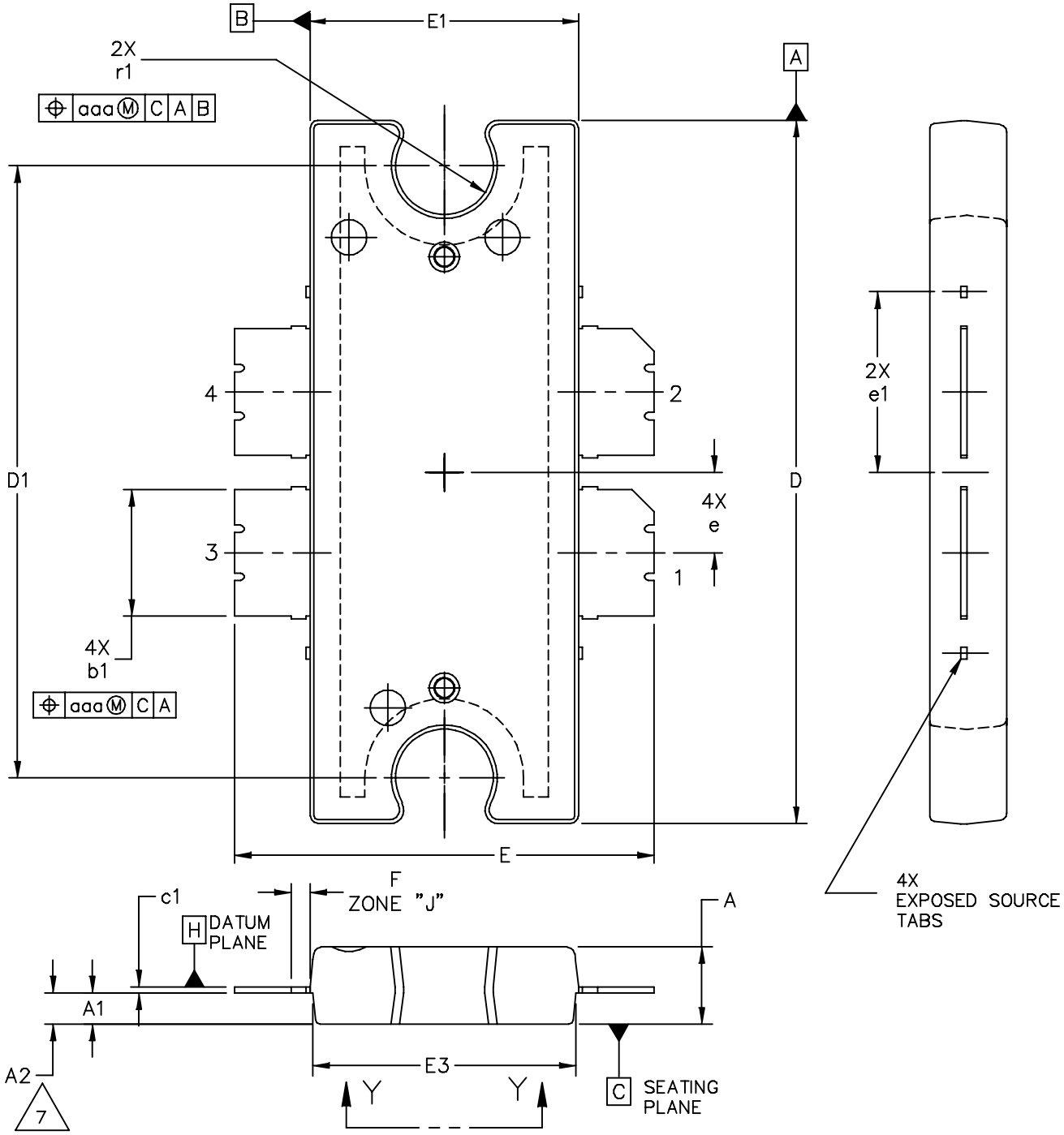

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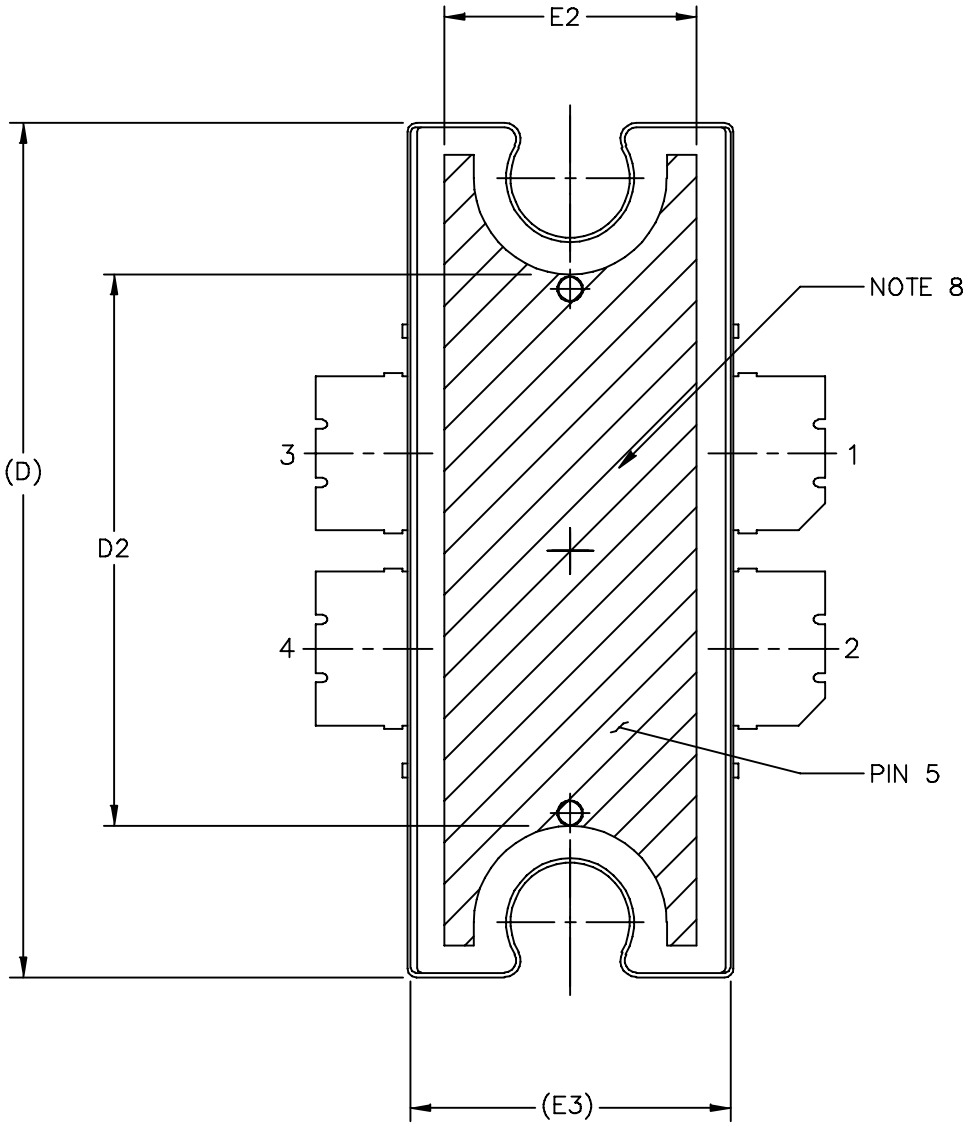
	STANDARD: NON−JEDEC	



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TITLE: TO−272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E
	CASE NUMBER: 1484−04	31 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: TO–272 4 LEAD WIDE BODY

DOCUMENT NO: 98ASA10575D | REV: E

CASE NUMBER: 1484–04 | 31 AUG 2007

STANDARD: NON–JEDEC

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
3	Jan. 2008	• Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table, related "Continuous use at maximum temperature will affect MTTF" footnote added and changed 200°C to 225°C in Capable Plastic Package bullet, p. 1 • Corrected V_{DS} to V_{DD} in the RF test condition voltage callout for $V_{GS(Q)}$, On Characteristics table, p. 2 • Updated Typical Performance table to provide better definition of characterization attributes, p. 3 • Updated PCB information to show more specific material details, Fig. 1, Test Circuit Schematic, p. 4 • Updated Part Numbers in Table 6, Component Designations and Values, to latest RoHS compliant part numbers, p. 4 • Adjusted scale for Fig. 8, Intermodulation Distortion Products versus Tone Spacing, to better match the device's capabilities, p. 7 • Replaced Fig. 12, MTTF versus Junction Temperature with updated graph. Removed $Amps^2$ and listed operating characteristics and location of MTTF calculator for device, p. 8 • Updated Fig. 13, CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal, to better represent production test signal, p. 8 • Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p.11-13. Added pin numbers 1 through 4 on Sheet 1. • Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 14-16. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations. • Added Product Documentation and Revision History, p. 17

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