LC898123AXD

CMOS LSI

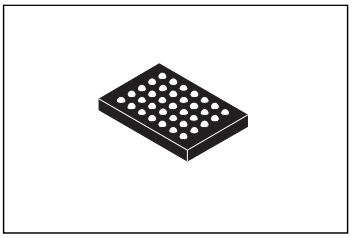
Optical Image Stabilization (OIS) / Auto Focus (AF) Controller & Driver

ON Semiconductor®

www.onsemi.com

Overview

LC898123AXD is a system LSI integrating an on-chip 32bit DSP, a Flash Memory and peripherals including analog circuits for Optical Image Stabilization (OIS) / Auto Focus (AF) control and H-bridge and constant current drivers.



WLCSP35, 3.39x2.3

Features

■ On-chip 32-bit DSP
- Built-in software digital servo filter
- Built-in Gyro filter

■ Flash Memory
- 12k Byte Flash memory to store data and DSP program

■ Peripherals
- AD converter
  - 12bit
  - Input 4ch
  - Equipped with a sample-hold circuit
- DA converter
  - 8bit
  - Output 3ch
- Built-in 2-wire Serial I/F circuit (with clock stretch function)
- Built-in Hall Bias circuit
- Built-in Hall Amp (Gain of Op-amp : ×6, ×12, ×50, ×75, ×100, ×150, ×200)
- Built-in OSC (Oscillator)
  - Typ. 41MHz (with Frequency adjustment function)
- Built-in LDO (Low Drop-Out regulator)
- Digital Gyro I/F for various types of gyro (SPI Bus)

■ Motor Driver
- OIS
  Constant current linear driver (×2ch, I_{full}=195mA)
  H-bridge driver (×2ch, Io max=220mA)
- OP-AF (unidirection)
  Constant current linear driver (×1ch, I_{full}=125mA)
- OP-AF (bidirection)
  Constant current linear driver (×1ch, I_{full}=120mA)
- CL-AF
  Constant current linear driver (×1ch, I_{full}=120mA)
  H-bridge driver (×1ch, Io max=150mA)

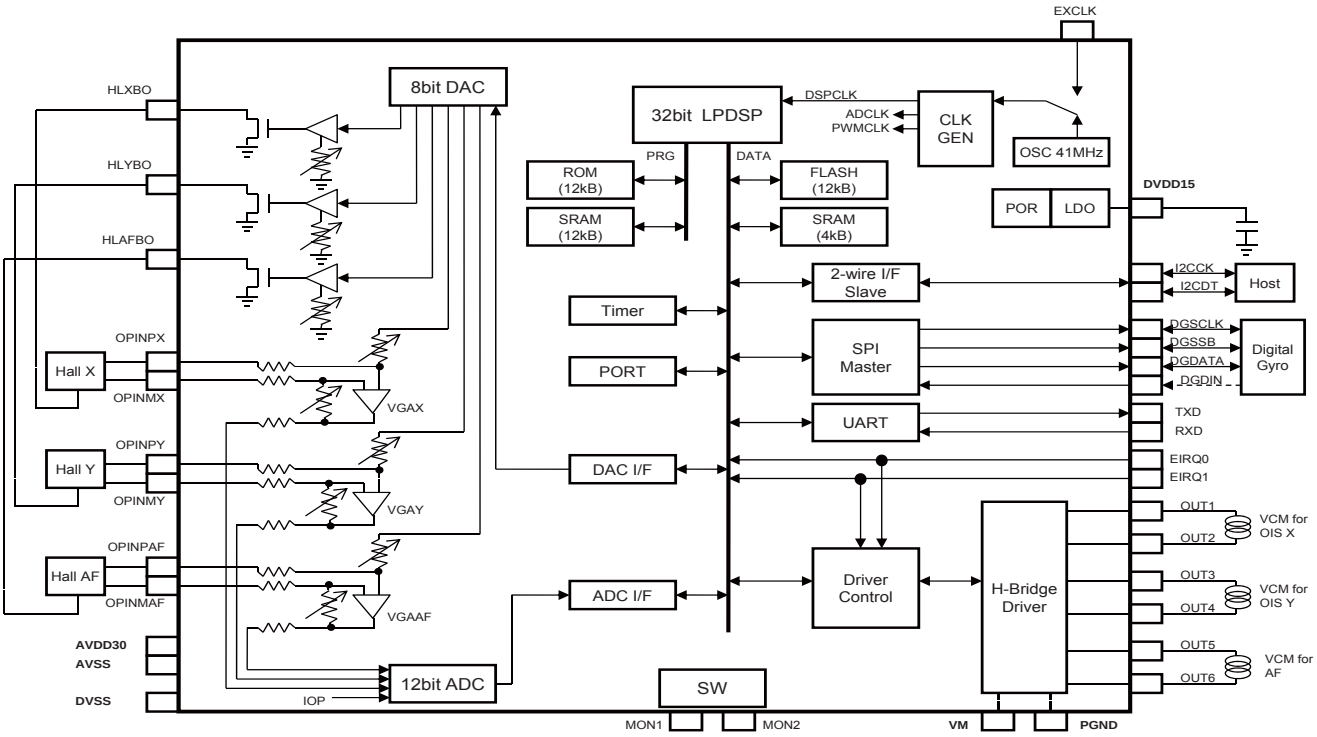
■ Package
- WLCSP35 (3.39mm × 2.3mm)
- Pb-Free / Halogen Free

■ Power Supply Voltage
- AD/DA/VGA/LDO/OSC : AVDD30=2.6V to 3.6V
- Digital I/O : AVDD30=2.6V to 3.6V
- Driver : VM=2.6V to 3.6V
- Core Logic : Generation by on-chip LDO DVDD15=1.5V (typ) output

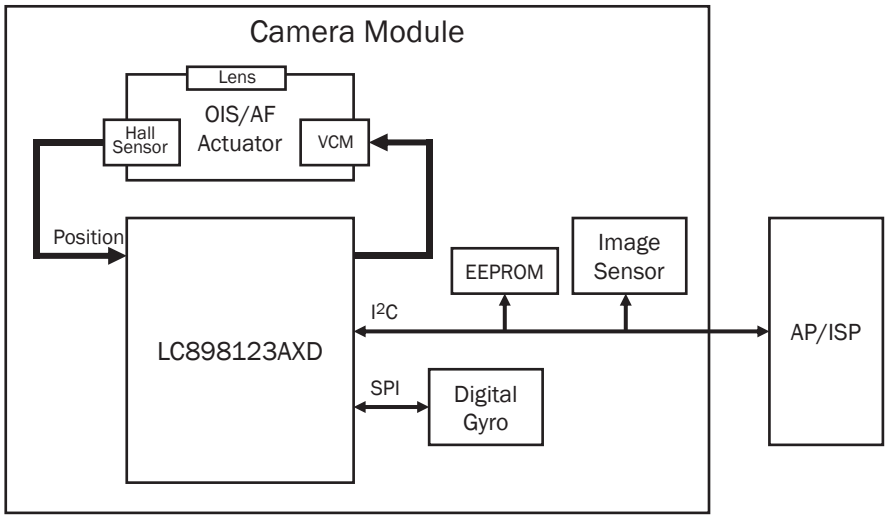
ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Block Diagram

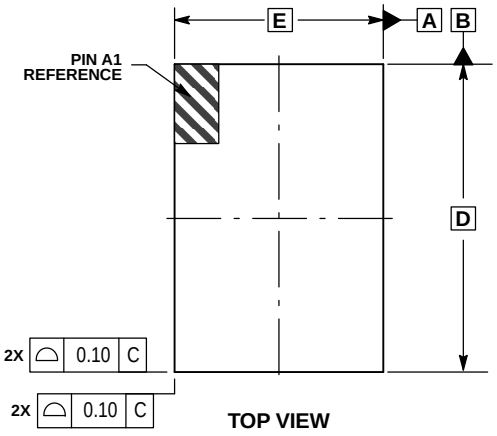


Application Diagram

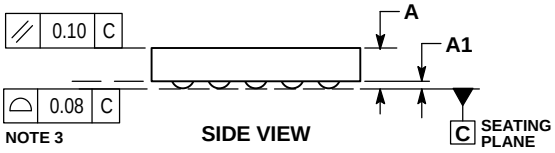


Package Dimensions
unit : mm

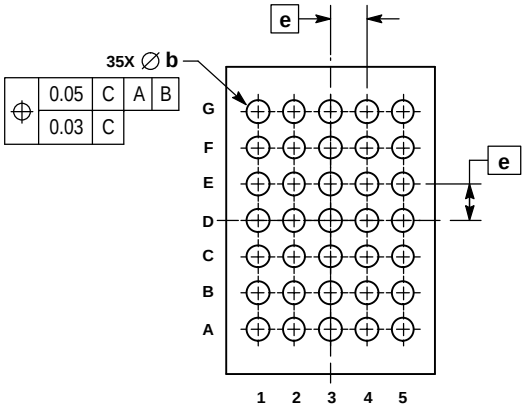
WLCSP35, 3.39x2.3
CASE 567JG
ISSUE O



TOP VIEW



SIDE VIEW

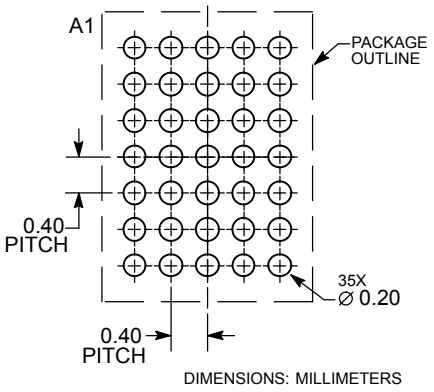


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.45
A1	0.03	0.13
b	0.15	0.25
D	3.39 BSC	
E	2.30 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment

Bottom View

	G	F	E	D	C	B	A
5	OUT5	OUT3	OUT4	PGND	OUT2	OUT1	WPB
4	OUT6	DGDATA	DGSSB	VM	I2CDT	I2CCK	TXD
3	HLAFBO	DGSCLK	DVSS	NC	EXCLK	DGDIN	EIRQ1
2	HLYBO	HLXBO	OPINMAF	OPINMX	OPINMY	EIRQ0	MON2
1	OPINPAF	OPINPX	OPINPY	AVSS	AVDD30	DVDD15	MON1

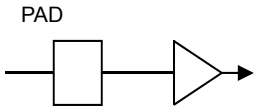
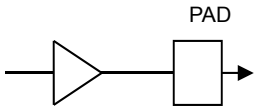
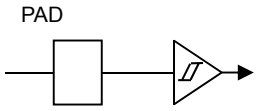
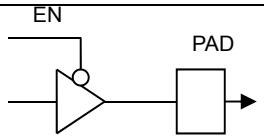
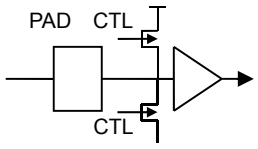
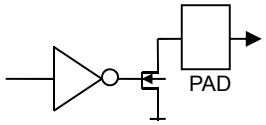
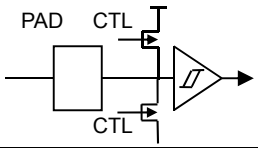
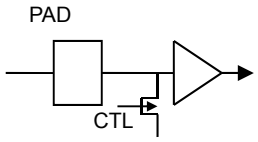
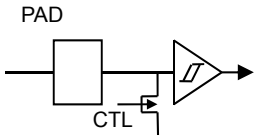
Driver

V_{DD} / V_{SS}

Internal Digital V_{DD} Output

Pin Description

I/O		Pin Specification			
I	Input	3IC	3V CMOS Input	3IA	3V Analog Input
O	Output	3IS	3V CMOS Schmitt Input	3OA	3V Analog Output
B	Bidirection	3ICUD	3V CMOS Input with PullUp/PullDown		
P	Power	3ISUD	3V CMOS Schmitt Input with PullUp/PullDown		
		3ICD	3V CMOS Input with PullDown		
		3ISD	3V CMOS Schmitt Input with PullDown		
		3O2	3V 2mA Output		
		3T2	3V 2mA TriState Output	Z/U/D	HiZ/PullUp/PullDown
		3OD	3V 2mA Open Drain Output	H/L	HIGH/LOW

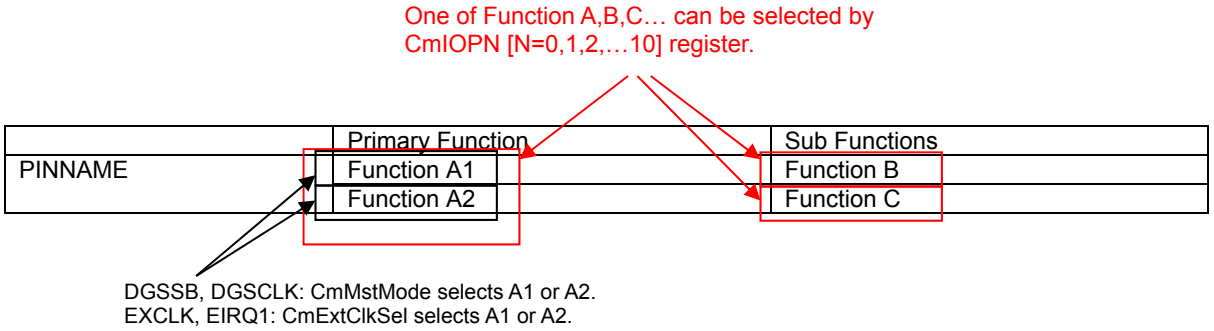
3IC	3V CMOS Input		3O2	3V 2mA Output	
3IS	3V Schmitt Input		3T2	3V 2mA TriState Output	
3ICUD	3V CMOS Input with PullUp/ Pulldown		3OD	3V 2mA Open Drain Output	
3ISUD	3V Schmitt Input with PullUp/ Pulldown				
3ICD	3V CMOS Input with Pulldown				
3ISD	3V Schmitt Input with Pulldown				

	Pin	I/O	I/O Spec		Primary Function	Sub Functions	Init
A1	MON1	B	3ICUD	3T2 3OA	(Debugger Data Output)	I2C Data I/O for DAC Monitor Servo Monitor Analog Out Internal Signal Monitor	L
A2	MON2	B	3ICUD	3T2 3OA	(Debugger Data Input)	I2C Data I/O for DAC Monitor Servo Monitor Analog Out Internal Signal Monitor	Z
A3	EIRQ1	B	3ISUD	3T2 3OA	External IRQ1 External Clock Input	I2C Data I/O for DAC Monitor UART Data Output(TXD) Internal Signal Monitor Servo Monitor Analog Input	Z
A4	TXD	B	3ICUD	3T2	UART Data Output	I2C Data I/O for DAC Monitor I2C Clock for I2C Slave Internal Signal Monitor	Z
A5	WPB	I	3ICD		Write Protect Input		-
B1	DVDD15	P			Internal LDO Power Output		-
B2	EIRQ0	B	3ICD	3OD	External IRQ0	I2C Data I/O for DAC Monitor UART Data Input(RXD) Internal Signal Monitor	Z
B3	DGDIN	B	3ICUD	3T2	Digital Gyro Data Input (4 Wired)	I2C Data I/O for DAC Monitor Internal Signal Monitor	U
B4	I2CCK	B	3IS	3OD	I2C Clock		Z
B5	OUT1	O		3OA	OIS Driver Output (H-Bridge or Linear)		-
C1	AVDD30	P			Analog Power (2.6 to 3.6V)		-
C2	OPINMY	I	3IA		OIS Hall Y Op-amp Input Minus		-
C3	EXCLK	B	3ISD	3OD	External Clock Input External IRQ1	I2C Data I/O for DAC Monitor Internal Signal Monitor	Z
C4	I2CDT	B	3IS	3OD	I2C Data		Z
C5	OUT2	O		3OA	OIS Driver Output (H-Bridge or Linear)		-
D1	AVSS	P			Analog GND		-
D2	OPINMX	I	3IA		OIS Hall X Op-amp Input Minus		-
D3	NC	-			No Connection		-
D4	VM	P			Driver Power (2.6V to 3.6V)		-
D5	PGND	P			Driver GND		-

	Pin	I/O	I/O Spec		Primary Function	Sub Functions	Init
E1	OPINPY	I	3IA		OIS Hall Y Op-amp Input Plus		-
E2	OPINMAF	I	3IA		AF Hall Op-amp Input Minus		-
E3	DVSS	P			Logic GND		-
E4	DGSSB	B	3ICUD	3T2	Digital Gyro I/F Chip Select Input	Digital Gyro I/F Chip Select Output	U
					Digital Gyro I/F Chip Select Output	Internal Signal Monitor	
E5	OUT4	O		3OA	OIS Driver Output (H-Bridge or Linear)		-
F1	OPINPX	I	3IA		OIS Hall X Op-amp Input Plus		-
F2	HLXBO	O		3OA	OIS Hall X Bias Output		-
F3	DGSCLK	B	3ICUD	3T2	Digital Gyro I/F Clock Input	Digital Gyro Clock Output	U
					Digital Gyro I/F Clock Output	I2C Clock for I2C Slave	
F4	DGDATA	B	3ICUD	3T2	Digital Gyro Data I/F Output (4 Wired)	Digital Gyro I/F Data I/O(3 Wired)	U
						I2C Data for I2C Slave	
F5	OUT3	O		3OA	OIS Driver Output (H-Bridge or Linear)		-
G1	OPINPAF	I	3IA		AF Hall Op-amp Input Plus		-
G2	HLYBO	O		3OA	OIS Hall Y Bias Output		-
G3	HLAFBO	O		3OA	AF Hall Bias Output		-
G4	OUT6	O		3OA	AF Driver Output (H-Bridge, Linear)		-
G5	OUT5	O		3OA	AF Driver Output (H-Bridge, Linear)		-

[How to select the function]

The initial function right after reset is set to be “Function A1” in the below table.
You can change the function by CmIOPN, CmMstMode, CmExtClkSel.



Electrical Characteristics

Logic

Absolute Maximum Rating at V_{SS}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	$V_{AD}30$ max	Ta ≤ 25°C	−0.3 to 4.6	V
Input/Output voltage	$V_{AI}30$, $V_{AO}30$	Ta ≤ 25°C	−0.3 to $V_{AD}30$+0.3	V
	$V_{DI}30$, $V_{DO}30$	Ta ≤ 25°C	−0.3 to $V_{AD}30$+0.3	V
Storage temperature	Tstg		−55 to 125	°C
Operating temperature	Topr		−30 to 85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ratings at Ta=−30 to 85°C, V_{SS}=0V

3.0V Power Supply ($AV_{DD}30$)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	$V_{AD}30$	2.6	2.8	3.6	V
Input voltage range	V_{IN}	0	-	$V_{AD}30$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

D.C. Characteristics at Input/Output V_{SS}= 0V, $AV_{DD}30$=2.6 to 3.6V, Ta =−30 to 85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable I/O
High-level input voltage	VIH	CMOS schmitt	1.48			V	3IS, 3ISUD, 3ISD
Low-level input voltage	VIL				0.37	V	
High-level input voltage	VIH	CMOS supported	1.40				3IC, 3ICUD, 3ICD
Low-level input voltage	VIL				0.51	V	
High-level output voltage	VOH	IOH=−2mA	$AV_{DD}30$ −0.4			V	3O2, 3T2
Low-level output voltage	VOL	IOL= 2mA			0.4	V	
Low-level output voltage	VOL	IOL= 2mA			0.2	V	3OD
Analog input voltage	VAI		AV_{SS}		$AV_{DD}30$	V	3IA
PullUp resistor	Rup		50		200	kΩ	3ICUD, 3ISUD
PullDown resistor	Rdn		50		220	kΩ	3ICUD, 3ISUD, 3ISD, 3ICD

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Non-volatile Memory Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Endurance	EN				1000	Cycles
Data retention	RT		10			Years

Driver

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Symbol
Power supply voltage	VM max		4.6	V
Output peak current	Iopeak	OUT1 to 4 T ≤ 10ms, ON-duty ≤ 20%	300	mA
		OUT5, OUT6 t ≤ 10ms, ON-duty ≤ 20%	200	mA
Output continuous current	Iomax	OUT1 to 4	220	mA
		OUT5, OUT6	150	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Range

Parameter	Symbol	Condition	Ratings	Symbol
Ambient temperature	Topg		−30 to +85	°C
Power supply voltage	VM		2.6 to 3.6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

H-Bridge Driver Output Characteristics at Ta=25°C, $AV_{DD}30$=VM=3.0V

Parameter	Symbol	Condition	Ratings (Ω)	Symbol
Output ON resistance OUT1 to OUT4	Ronu	Io=220mA (Pch)	1.1	Ω
	Rond	Io=220mA (Nch)	1.3(*)	Ω
Output ON resistance OUT5, OUT6	Ronu	Io=150mA (Pch)	1.5	Ω
	Rond	Io=150mA (Nch)	1.4(*)	Ω

(*) include Constant current detect resistance

Constant Current Driver Output at Ta=25°C, $AV_{DD}30$=VM=2.8V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1 to OUT4	I_{full}	OIS_DA[10:0]=7FFh OIS_DB[10:0]=7FFh	185.5	195.0	205.0	mA
Output Current OUT5, OUT6		OP-AF(unidirection) AF_D[9:0]=3FFh		125.0		mA
		OP-AF(bidirection) CL-AF AF_D[9:0]=3FFh		120.0		mA
Compliance Voltage OUT1 to OUT4	Vcomp		0.4			V
Compliance Voltage OUT5,OUT6		OP-AF(unidirection)	0.4			V
		OP-AF(bidirection) CL-AF	0.5			V

Total output current is less than 500mA.

OP-AF (unidirection)

VCM registance (Rvcm) = (VM − Vcomp)/Io [Ω]

OP-AF (bidirection) / CL-AF / OIS

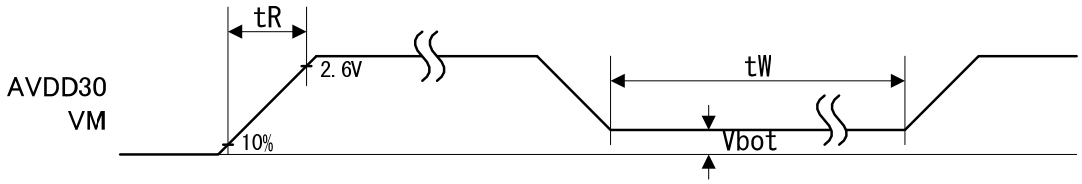
VCM registance (Rvcm) = (VM − (Ronu × Io+Vcomp))/Io [Ω]

Output ON resistance (Ron) = VM / Io – Rvcm [Ω]

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

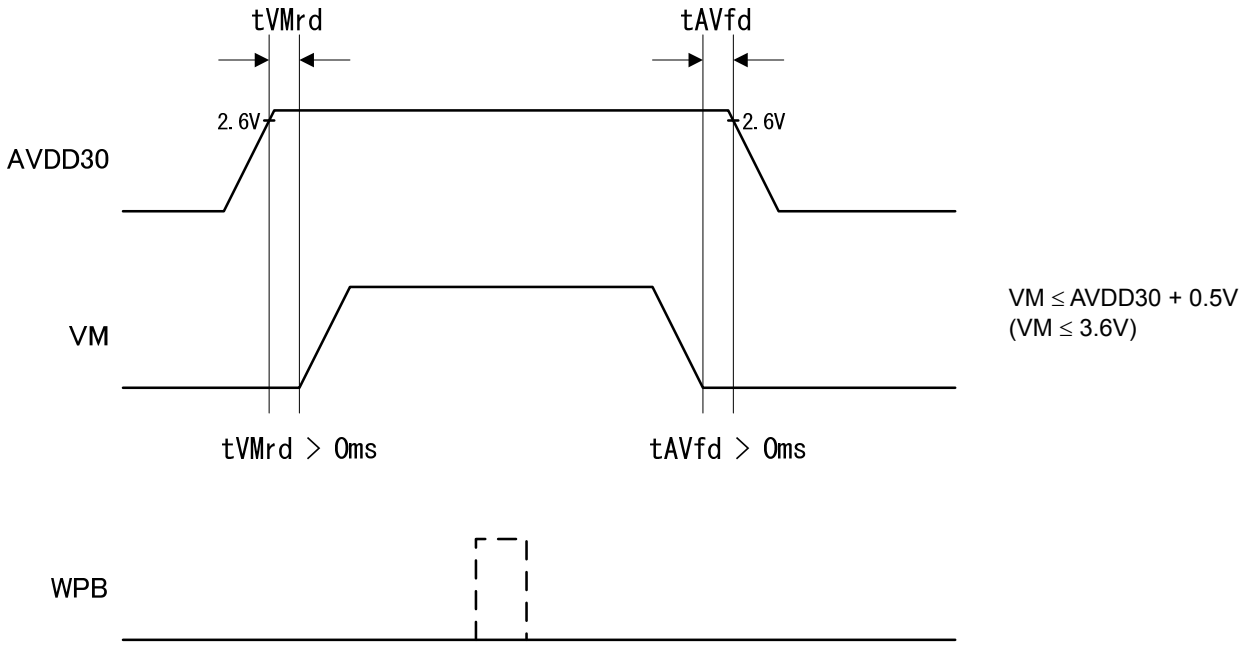
AC Characteristics

Power Sequence



Item	Symbol	Min	Typ	Max	Units
Rise time	tR			5	ms
Wait time	tW	100			ms
Bottom Voltage	Vbot			0.2	V

Injection order between AVDD30 and VM is below.



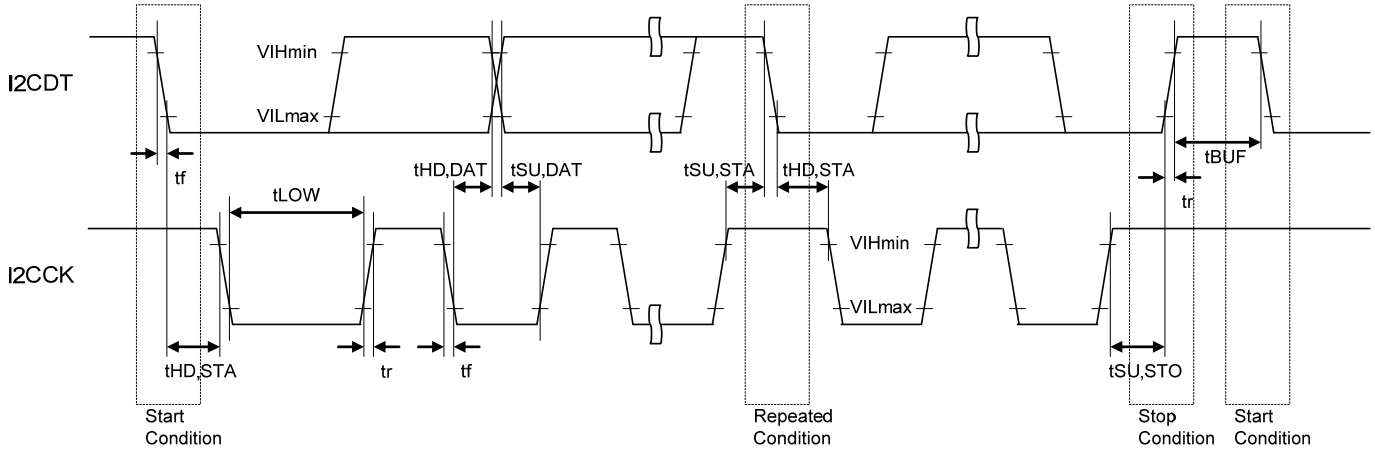
VM ≤ AVDD30 + 0.5V
(VM ≤ 3.6V)

WPB must be open or pull down normally. When Erase or Program is made to Flash, WPB have to be High.
Before power off of AVDD, Flash I/F must reset and OSC must set to standby.
I2CDT,I2CCK,EXCLK and EIRQ0 tolerate 3V input at the time of power off.

The data in the flash memory may be rewrited if you do not keep specifications.
And it is forbidden to power off during flash access. The data in the flash memory may be rewrited.

2-wire serial Interface Timing

The communication protocol is compatible with I^2C (Fast mode Plus). This circuit has clock stretch function.



I^2C interface timing definition

Item	Symbol	Pin name	Min	Typ	Max	Units
SCL clock frequency	Fscl	I2CCK			1000	kHz
START condition hold time	tHD,STA	I2CCK I2CDT	0.26			μs
SCL clock Low period	tLOW	I2CCK	0.5			μs
SCL clock High period	tHIGH	I2CCK	0.26			μs
Setup time for repetition START condition	tSU,STA	I2CCK I2CDT	0.26			μs
Data hold time	tHD,DAT	I2CCK I2CDT	0 (*1)		0.9	μs
Data setup time	tSU,DAT	I2CCK I2CDT	50			ns
SDA, SCL rising time	tr	I2CCK I2CDT			120	ns
SDA, SCL falling time	tf	I2CCK I2CDT			120	ns
STOP condition setup time	tSU,STO	I2CCK I2CDT	0.26			μs
Bus free time between STOP and START	tBUF	I2CCK I2CDT	0.5			μs

(*1) Although the I^2C specification defines a condition that 300 ns of hold time is required internally, LC898123AXD is designed for a condition with typ. 100 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898123AXD-VH	WLCSP35, 3.39x2.3 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF