

# 1.5V Drive Nch+Pch MOSFET

## US6M11

### ●Structure

Silicon N-channel MOSFET /  
Silicon P-channel MOSFET

### ●Features

- 1) Nch MOSFET and Pch MOSFET are put in TUMT6 package.
- 2) Low on-resistance.
- 3) Low voltage drive (1.5V drive).
- 4) Built-in G-S Protection Diode.

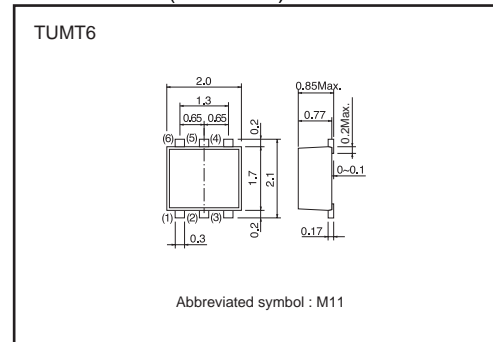
### ●Applications

Switching

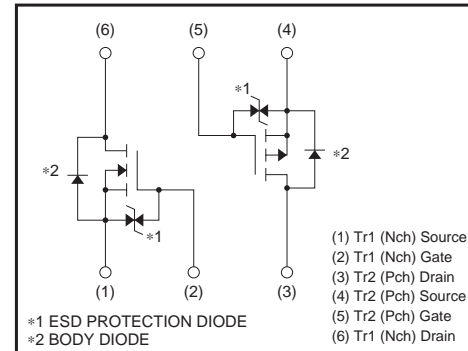
### ●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6M11		○

### ●Dimensions (Unit : mm)



### ●Inner circuit



### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit	
		Tr1 : Nchannel	Tr2 : Pchannel		
Drain-source voltage	V <sub>DSS</sub>	20	-12	V	
Gate-source voltage	V <sub>GSS</sub>	±10	±10	V	
Drain current	Continuous	I <sub>D</sub>	±1.5	±1.3	A
	Pulsed	I <sub>DP</sub> *1	±6	±5.2	A
Source current (Body diode)	Continuous	I <sub>S</sub>	0.5	-0.5	A
	Pulsed	I <sub>SP</sub> *1	6	-5.2	A
Power dissipation	P <sub>D</sub> *2	1.0		W / TOTAL	
		0.7		W / ELEMENT	
Channel temperature	T <sub>ch</sub>	150		°C	
Range of storage temperature	T <sub>stg</sub>	-55 to +150		°C	

\*1 P<sub>w</sub>≤10μs, Duty cycle≤1%

\*2 Mounted on a ceramic board.

### ●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	R <sub>th(ch-a)</sub> *2	125	°C/W / TOTAL
		179	°C/W / ELEMENT

\*2 Mounted on a ceramic board

## &lt;N-ch&gt;

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	20	–	–	V	I <sub>D</sub> = 1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	1	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	0.3	–	1.0	V	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1mA
Static drain-source on-state resistance	R <sub>DS(on)*</sub>	–	130	180	mΩ	I <sub>D</sub> = 1.5A, V <sub>GS</sub> = 4.5V
		–	170	240	mΩ	I <sub>D</sub> = 1.5A, V <sub>GS</sub> = 2.5V
		–	220	310	mΩ	I <sub>D</sub> = 0.8A, V <sub>GS</sub> = 1.8V
		–	300	600	mΩ	I <sub>D</sub> = 0.3A, V <sub>GS</sub> = 1.5V
Forward transfer admittance	Y <sub>fs</sub>  *	1.6	–	–	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1.5A
Input capacitance	C <sub>iss</sub>	–	110	–	pF	V <sub>DS</sub> = 10V
Output capacitance	C <sub>oss</sub>	–	18	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	15	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)*</sub>	–	5	–	ns	V <sub>DD</sub> ≐ 10V
Rise time	t <sub>r</sub> *	–	5	–	ns	I <sub>D</sub> = 1A
Turn-off delay time	t <sub>d(off)*</sub>	–	20	–	ns	V <sub>GS</sub> = 4.5V
Fall time	t <sub>f</sub> *	–	3	–	ns	R <sub>L</sub> ≐ 10Ω
Total gate charge	Q <sub>g</sub> *	–	1.8	–	nC	V <sub>DD</sub> ≐ 10V, V <sub>GS</sub> = 4.5V
Gate-source charge	Q <sub>gs</sub> *	–	0.3	–	nC	I <sub>D</sub> = 1.5A
Gate-drain charge	Q <sub>gd</sub> *	–	0.3	–	nC	R <sub>L</sub> ≐ 6.7Ω, R <sub>G</sub> = 10Ω

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	1.2	V	I <sub>S</sub> = 1.5A, V <sub>GS</sub> =0V

\*Pulsed

## &lt;P-ch&gt;

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	–12	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –12V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–0.3	–	–1.0	V	V <sub>DS</sub> = –6V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)*</sub>	–	190	260	mΩ	I <sub>D</sub> = –1.3A, V <sub>GS</sub> = –4.5V
		–	280	390	mΩ	I <sub>D</sub> = –0.6A, V <sub>GS</sub> = –2.5V
		–	400	600	mΩ	I <sub>D</sub> = –0.6A, V <sub>GS</sub> = –1.8V
		–	530	1060	mΩ	I <sub>D</sub> = –0.2A, V <sub>GS</sub> = –1.5V
Forward transfer admittance	Y <sub>fs</sub>  *	1.4	–	–	S	V <sub>DS</sub> = –6V, I <sub>D</sub> = –1.3A
Input capacitance	C <sub>iss</sub>	–	290	–	pF	V <sub>DS</sub> = –6V
Output capacitance	C <sub>oss</sub>	–	28	–	pF	V <sub>GS</sub> = 0V
Reverse transfer capacitance	C <sub>rss</sub>	–	21	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)*</sub>	–	8	–	ns	V <sub>DD</sub> ≐ –6V
Rise time	t <sub>r</sub> *	–	10	–	ns	I <sub>D</sub> = –0.6A
Turn-off delay time	t <sub>d(off)*</sub>	–	30	–	ns	V <sub>GS</sub> = –4.5V
Fall time	t <sub>f</sub> *	–	9	–	ns	R <sub>L</sub> ≐ 10Ω
Total gate charge	Q <sub>g</sub> *	–	2.4	–	nC	V <sub>DD</sub> ≐ –6V, V <sub>GS</sub> = –4.5V
Gate-source charge	Q <sub>gs</sub> *	–	0.6	–	nC	I <sub>D</sub> = –1.3A
Gate-drain charge	Q <sub>gd</sub> *	–	0.4	–	nC	R <sub>L</sub> ≐ 4.6Ω, R <sub>G</sub> = 10Ω

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	–1.2	V	I <sub>S</sub> = –1.3A, V <sub>GS</sub> =0V

\*Pulsed

●Electrical characteristic curves

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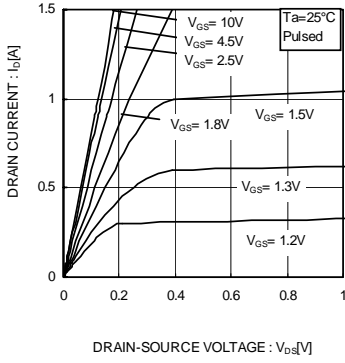


Fig.1 Typical Output Characteristics( I )

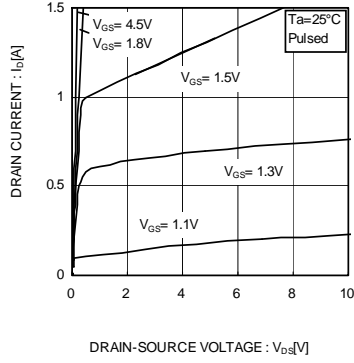


Fig.2 Typical Output Characteristics( II )

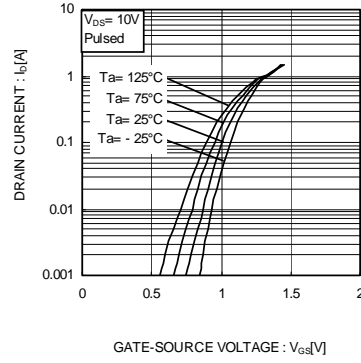


Fig.3 Typical Transfer Characteristics

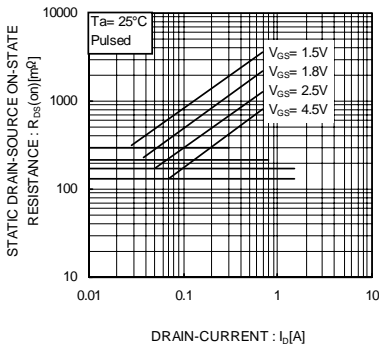


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current( I )

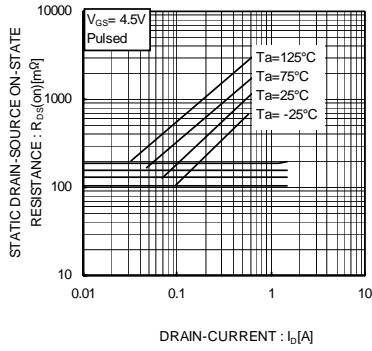


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current( II )

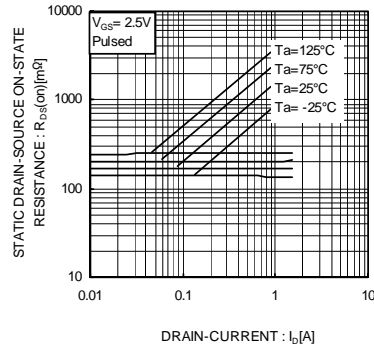


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current( III )

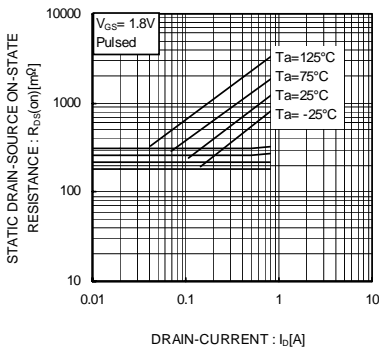


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current( IV )

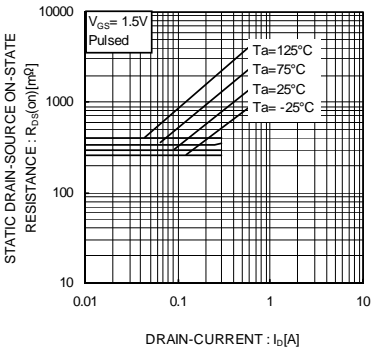


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current( V )

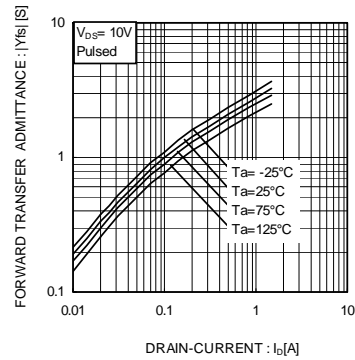


Fig.9 Forward Transfer Admittance vs. Drain Current

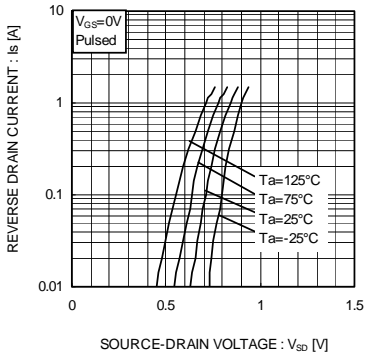


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

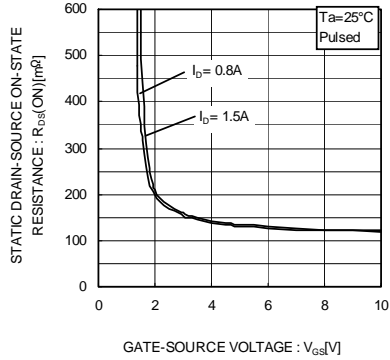


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

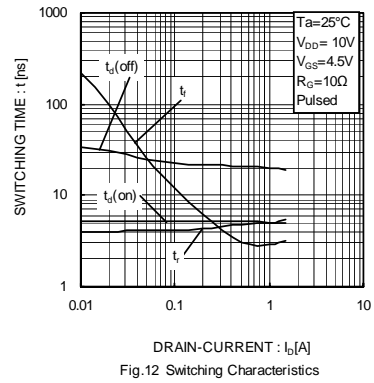


Fig.12 Switching Characteristics

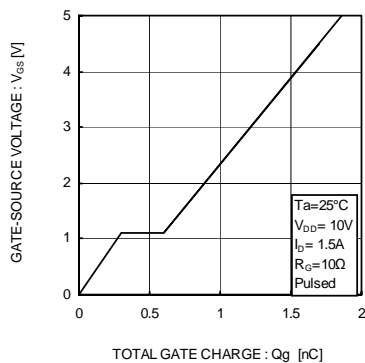


Fig.13 Dynamic Input Characteristics

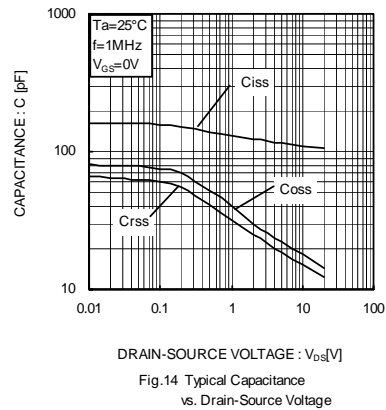


Fig.14 Typical Capacitance vs. Drain-Source Voltage

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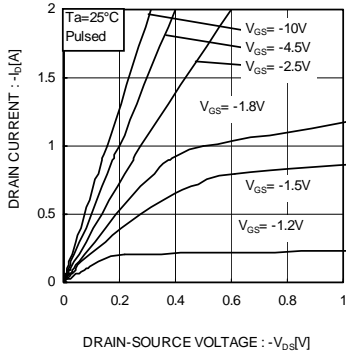


Fig.1 Typical output characteristics ( I )

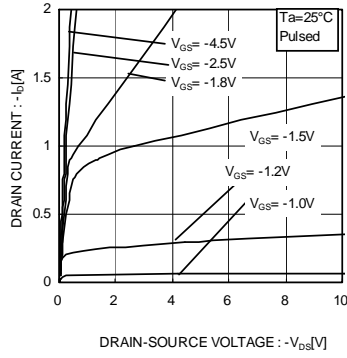


Fig.2 Typical output characteristics ( II )

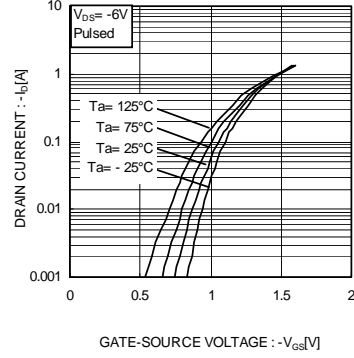


Fig.3 Typical Transfer Characteristics

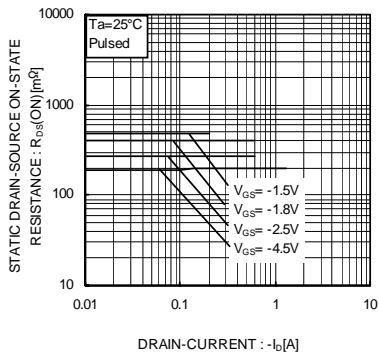


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current ( I )

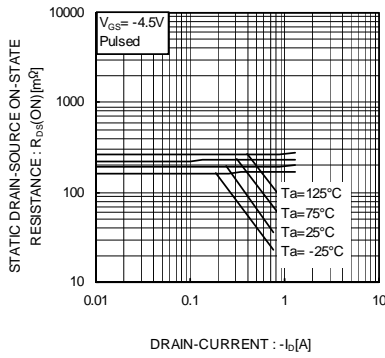


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current ( II )

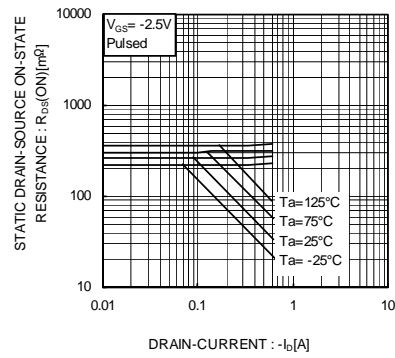


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

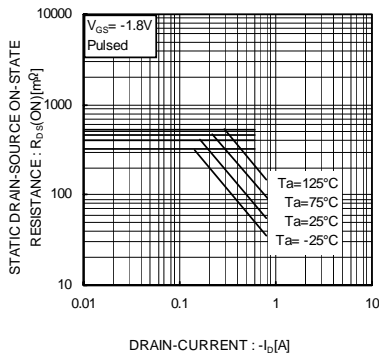


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

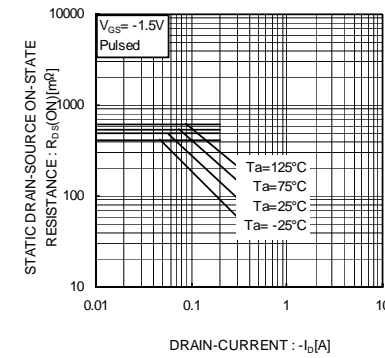


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (IV)

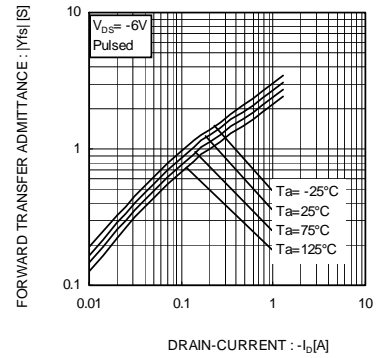
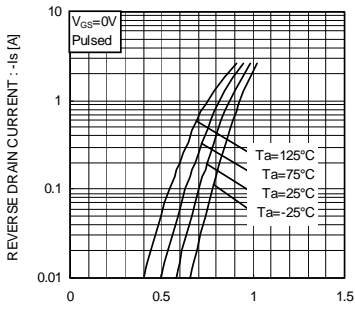
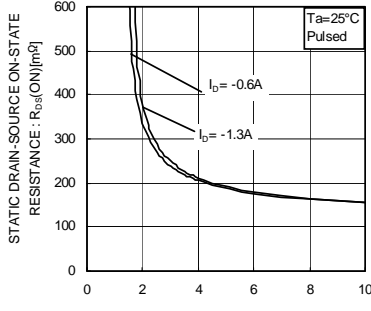


Fig.9 Forward Transfer Admittance vs. Drain Current



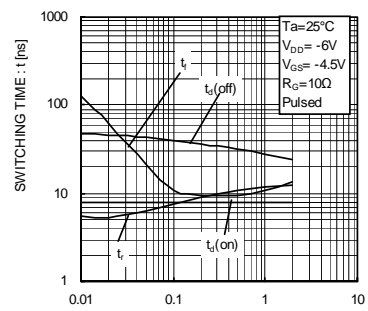
SOURCE-DRAIN VOLTAGE :  $-V_{DS}$  [V]

Fig.10 Reverse Drain Current vs. Source-Drain Voltage



GATE-SOURCE VOLTAGE :  $-V_{GS}$  [V]

Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage



DRAIN-CURRENT :  $-I_D$  [A]

Fig.12 Switching Characteristics

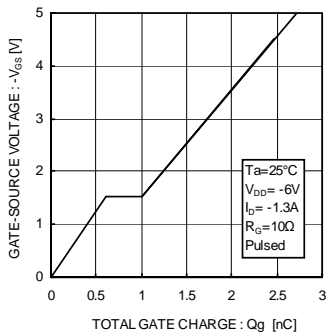


Fig.13 Dynamic Input Characteristics

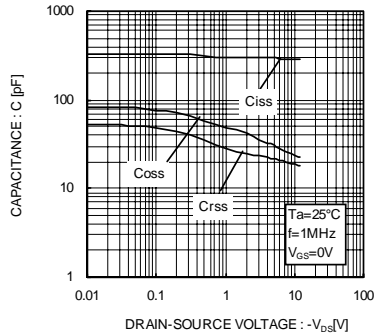


Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuit

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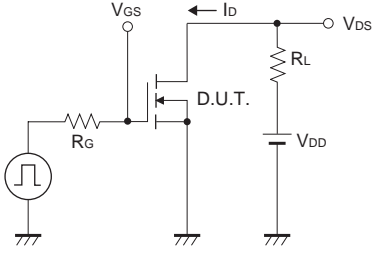


Fig.1-1 Switching Time Measurement Circuit

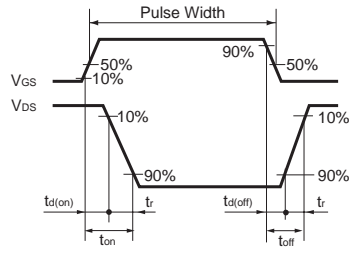


Fig.1-2 Switching Waveforms

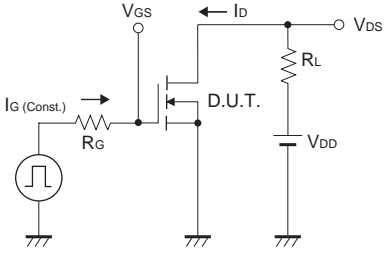


Fig.2-1 Gate Charge Measurement Circuit

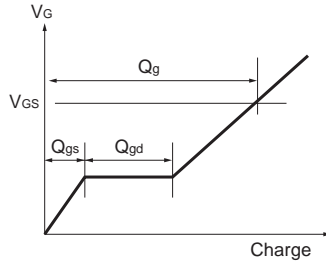


Fig.2-2 Gate Charge Waveform

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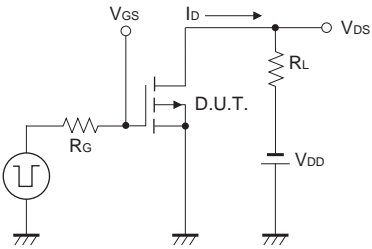


Fig.3-1 Switching Time Measurement Circuit

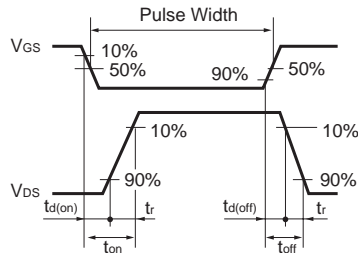


Fig.3-2 Switching Waveforms

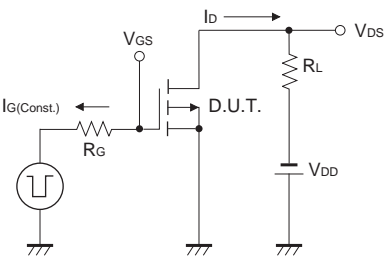


Fig.4-1 Gate Charge Measurement Circuit

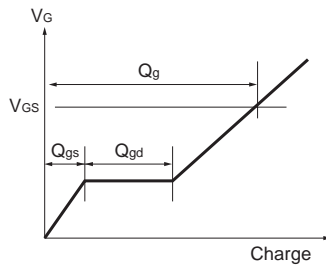


Fig.4-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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