**Freescale Semiconductor**
User Guide

AP52233UG
Rev. 5, 03/2008

# Application Module Student Learning Kit Users Guide featuring the Freescale ColdFire® M52233

**For use with the following part numbers:**
**AP52233SLK**
**PB52233SLK**
**AP52233SLK**

Design and/or Manufacturing services for this board provided by:

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# REVISION

| Date | Rev | Comments |
|---|---|---|
| March 16, 2006 | 0 | Initial Release. |
| April 26, 2006 | 1 | Updated Getting Started Section. Corrected EMC classification |
| September 25, 2006 | 2 | Modified Getting Started section to point to Hands-On Seminar documentation from Freescale. |
| July 16, 2007 | 3 | Removed reference document revision details. |
| November 1, 2007 | 4 | Reformatted |
| February 26, 2008 | 5 | Fixed Diagram |

## CAUTIONARY NOTES

- Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

- Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

- EMC Information on the AP52233SLK board:

  a) This product, as shipped from the factory with associated power supplies and cables, has been verified to meet with **FCC** requirements as a **CLASS A** product.

  b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

  c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

  d) Attaching additional wiring to this product or modifying the product operation from the factory configuration may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

## TERMINOLOGY

This development board uses option selection jumpers. A jumper is a plastic shunt that connects 2 terminals electrically. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

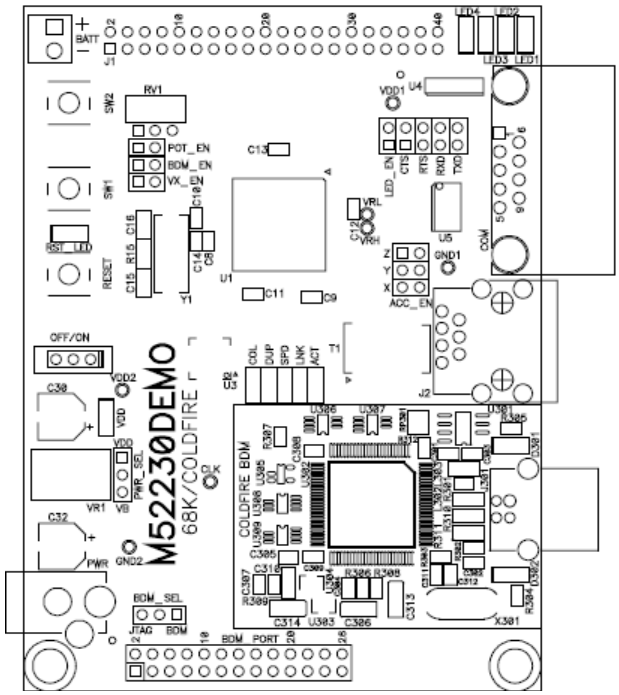
Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a razor knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Throughout this document, where used, the name AP52233SLK applies equally to the AP52233SLK, AP52233SLK, and PB52233SLK product names.

# FEATURES

The AP52233SLK is a low-cost development system for the Freescale MCF52233 ColdFire microcontroller. Application development is quick and easy with the included DB9 serial cable, and integrated BDM. CodeWarrior Development Tools are also provided to support application development and debug. The integrated BDM allows easy application development and debugging. An optional BDM port compatible with standard ColdFire BDM / JTAG interface cables and hosting software is provided but not installed.

- MCF52233 CPU, 80 pins
  - 256 Byte Flash
  - 32K Byte Ram
  - DMA Controller w/ Timers
  - Programmable Interrupt Timer
  - 8ch, 12b ADC
  - QSPI, IIC, and CAN Serial Ports
  - Fast Ethernet Controller (FEC) and Ethernet
  - Phy (ePHY)
  - 3 x UART Serial Ports with DMA capability
  - 4 GPT Timers
  - BDM / JTAG Port
  - 3.3V operation
  - 60 MHz Internal Bus
- 40 pin I/O port
- Ethernet port
- Integrated USB BDM port
- BDM / JTAG Port (not installed)
- RS-232 Serial Port w/ DB9-S Connector
- External XTAL, 25 MHz
- ON/OFF Power Switch w/ LED indicator
- RESET switch w/ indicator
- Power Input Selection Jumper
  - Power Input from USB BDM
  - Power Input from on-board, +3.3V, regulator
  - Power Input from terminal block
  - Power from connector J1
  - Optional Power output through connector J1
- User Features
  - 3-axis Accelerometer
  - 4 User LED's w/ enable
  - 2 User Push Switches
  - 5k ohm POT w/ enable
- Option Jumpers
  - Power Input Select
  - Optional Power Output Enable
  - BDM_EN
  - XTAL_EN
  - POT_EN
  - COM_EN
  - LED_EN




- Connectors
  - RJ-45 Ethernet Connector
  - Type B USB Connector
  - DB9 Serial Connector
  - 2.0mm Barrel Power Input
  - 2pos, screw type, terminal block

Supplied with DB9 Serial Cable, USB cable, Ethernet Cable, Support CD, and CodeWarrior Development Studio CD

Board Size 3.0" x 4.3"
Power Input: +5VDC to +15VDC, 9VDC typical

# REFERENCES

Reference documents are provided on the support CD in Acrobat Reader format. Visit www.freescale.com for current documentation and support materials.

| | |
|---|---|
| AP52233SLKUG.pdf | AP52233SLK User Guide (this document) |
| HCS52233SCHEMSLKREVC.pdf | AP52233SLK Board Schematic, Rev. C |

# INTRODUCTION

Before using this module, the user should be familiar with the hardware and software operation of the target MCU. Refer to the M52233 User Manual and M52233 Reference Manual for details on MCU operation. The module's purpose is to promote the features of the M52233 and to assist the user in quickly developing an application in a known working environment. Users should be familiar with memory mapping, memory types, and embedded software design for quick, successful, application development.

The AP52233SLK application module is a fully assembled, fully functional module supporting Freescale M52233 microcontroller for educational use. The module comes with a integrated USB Background Debug Mode (BDM), and USB cable for stand-alone operation. Support software for this module is provided for Windows 95/98/NT/2000/XP operating systems.

# GETTING STARTED

The AP52233SLK ships from the factory with a USB stack and open-source RTOS from InterNicheTechnologies preloaded. Refer to the Hands-On Workshop: Dynamic Web Page Server with MCF5223x Family (AX131.pdf) on the Axiom Support CD for details on how to get started quickly. Table 1 below shows the default jumper configuration for the AP52233SLK.

**Table 1: Default Jumper Configuration**

| PWR_SEL | CONFIGURATION: |
|---|---|
| VB VDD  | Select power input from integrated USB-BDM |

| | | |
|---|---|---|
|  | POT_EN | POT_EN must be installed |
|  | BDM_EN | BDM_EN are "don't care" and may be left on or taken off |
|  | VX_EN | VX_EN are "don't care" and may be left on or taken off |

| | | |
|---|---|---|
|  | LED_EN | Enable user LED's |
|  | CTS | CTS and RTS are "don't care" |
|  | RTS | |
|  | RxD | Enable RS-232 Communications RX |
|  | TxD | Enable RS-232 Communications TX |

# OPERATION

## *POWER*

The AP52233SLK is designed to allow application development while powered from the USB_BDM. A 2.0mm barrel connector and a 2-position, screw-type, terminal block (BATT) has been applied to support stand-alone operation. The board may also be powered through connector J1. Additionally, the board may be configured to supply power through connector J1 to external circuitry. An OFF/ON switch allows the user to quickly and easily connect and disconnect all power sources.

When using the integrated USB-BDM, the board draws power from the USB bus. Excessive current drain will violate the USB specification causing the USB bus to disconnect forcing a POR. Total current consumption of the board and connected circuitry, therefore, must be less than **500mA**.

> **CAUTION:** Violating the USB specification will cause the USB bus to disconnect. This will force a hard reset on the target.

The installed barrel connector accepts a center-positive, 2.1m barrel plug. The terminal block accepts wire sizes ranging from 28ga to 16ga. Voltage input must be in the range between +5V and +15V. At no time should input voltage exceed +15V as damage to the board may result. The terminal block input is connected directly to the upper voltage rail. Input protection is not applied on this voltage input. The user must exercise caution when using the terminal block to input power to the board.

Voltage supplied through connector J1 is also connected directly to the board voltage rails. No protection is applied on this input and the user must exercise caution when powering the board from connector J1.

> **CAUTION:** Input protection is **NOT** applied to the J1 or BATT power inputs. Excessive input voltage or current will damage the board.

## *POWER JACK*

The PWR power jack consists of a 2.1mm, center-positive, barrel connector. Voltage applied at this connector should range between +5V and +15V.

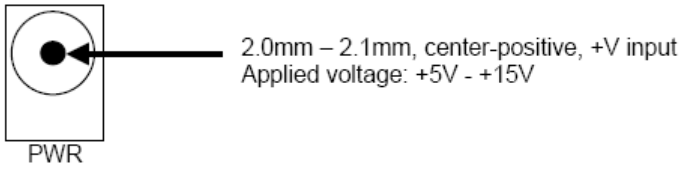
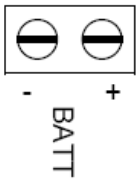



**Figure 1: PWR Jack**

## *TERMINAL BLOCK*

The BATT terminal block is a 3.5mm, screw-type terminal block connected directly to the VDD voltage rail. This allows the use of 2 AA batteries to supply power to the board. Exercise caution when using this input since input protection is not applied. This input requires a regulated +3.3V voltage source.




Accepts wire size 28AWG – 16AWG
Applied voltage must be +3.3V.

**Figure 2: BATT Terminal Power Block**

## *Connector J1*

See the schematic for details on using this connection to supply power to the board or source power from the board. This input requires a regulated +3.3V voltage source.

**CAUTION:** Do not over drive either the J1 or BATT inputs as damage to the board may result.

## *VDD LED*

The VDD LED indicates the state of power applied to the development board. The VDD LED is located on the output of the OFF/ON switch. This LED will light when the board is energized regardless of power input source.

## *POWER SWITCH*

The OFF/ON switch connects and disconnects all input sources to the upper voltage rail. In the OFF position, the board is unpowered and no voltage is present. In the ON position, the input voltage source is connected to the upper voltage rail.

ON/OFF CONFIGURATION:

O
F
F

O
N

OFF – Input power source disconnected from upper voltage rail.
ON – Input power source connected to upper voltage rail

**Figure 3: ON/OFF Switch**

## *POWER SELECT*

Configuration of applied input power is controlled using 2 option headers. The PWR_SEL header selects between the on-board voltage regulator and the USB voltage input. The VX_EN header connects J1-1 directly to the upper voltage rail. The illustrations below show the different configuration for each option header.

## *PWR_SEL*

Power from the integrated BDM is drawn from the USB bus and is limited to **500mA**. Excessive current drain will violate the USB specification causing the USB bus to disconnect.

> **CAUTION:** Violating the USB specification will cause the USB bus to disconnect. This will cause the board to reset.

The on-board voltage regulator (VR1) accepts power input through a 2.1mm barrel connector (PWR). Input voltage may range from +5V to +15V. VR1 provides a +3.3V fixed voltage output with output current limited to 800mA. Over-temperature and over-current limit built into the voltage regulator provides limited protection from damage due to excessive stresses.

The user should consider the maximum output current of the selected power source when attempting to power off-board circuitry through connector J1.

PWR_SEL CONFIGURATION:

VB VDD

Select power input from USB-BDM

PWR_SEL

VB VDD

Select power input from VR1

**Figure 4: PWR_SEL Option Header**

## *VX_EN*

The VX_EN option header is a 2-pin jumper that connects the target board voltage rail to J1-1. J1-3 is connected directly to the ground plane. Use of this feature requires a regulated +3.3V

input power source. This power input is decoupled to minimize noise input but is not regulated. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if over-driven. Also, do not attempt to power the target board through this connector while also applying power through the USB-BDM or the PWR connector; damage to the board may result.

Power may be sourced to off-board circuitry through the J1 connector. The current limitation of the USB bus or the on-board regulator must be considered when attempting to source power to external circuitry.

Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. The figure below details the VX_EN option header connections.

**ON** Enable power connection to connector J1

VX_EN

**OFF** Disable power connection to connector J1

VX_EN

**Figure 5: VX_EN Option Header**

**CAUTION:** Do not apply power to connector J1 while also sourcing power from either the PWR connector or the USB-BDM circuit. Damage to the board may result.

**NOTE:** Do not exceed available current supply from the USB-BDM cable or on-board regulator when sourcing power through connector J1 to external circuitry.

## *RESET*

The MCF52233 can be reset several ways. A logic low applied to the RSTI* input will force the device into RESET. This input is used by the RESET pushbutton. This input is also used to force the device in to BDM mode. An internal low-voltage detect forces the part into RESET when voltage falls too low.

## *RESET SWITCH*

The RESET switch provides a method to apply an asynchronous reset to the MCU and is connected directly to the RSTI* input on the MCU. Pressing the RESET switch forces RSTI* input low until the switch is released. An external pull-up on the RSTI* line prevents spurious resets and allowing normal operation.

## *LOW VOLTAGE DETECT*

The MCF52233 utilizes an internal Low Voltage Detect (LVD) to protect against under-voltage conditions. The LVD is enabled out of RESET. Consult the MCF52233 Device User Guide for details on configuring LVD operation.

## *RESET INDICATOR*

The RST_LED is connected to the RSTO* output on the MCF52233. This LED lights when the MCU is in RESET and remains on for the duration of an asserted RSTO* signal. RSTO* may also be used as a GP output to drive the RST_LED indicator as needed.

## *LOW POWER MODES*

The MCF52233 supports several operational modes designed to reduce power consumption. Low-power modes include Wait, Doze, Stop, and Halt. Refer to the MCF52235 documentation at www.freescale.com for details on configuring and using the various low-power modes.

## *TIMING*

Timing to the AP52233SLK clock module is provided by an external, 25 MHz crystal oscillator.

Refer to the MCF52235 documentation at www.freescale.com for details on use and configuration.

## *COMMUNICATIONS*

The AP52233SLK board provides 2 SCI ports, 1 QSPI port, and 1 IIC port. RS-232 communication is supported through a DB9 (COM) connector and through connector J1. QSPI and IIC communications are supported only through connector J1. The COM_EN option header enables SCI0 functionality between the MCU and the COM connector.

## *SCI Port*

An RS-232 transceiver provides RS-232 to TTL/CMOS logic level translation between the COM connector and the MCU. The COM connector is a 9-pin D-sub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD0 and RXD0 are routed from the transceiver to the MCU. These signals are also available on connector J1. Hardware flow control signals RTS0 and CTS0 are available on connector J1. RTS has been biased for correct 2-wire operation.

SCI1 signals are available on connector J1 and route directly between the MCU and connector J1. No RS-232 logic-level translation is provided on SCI1 signals.

## COM_EN

The COM_EN option header individually connects and disconnects SCI0 signals between the MCU and the SCI transceiver. Removing a shunt disconnects the associated signal. Install a shunt connects the associated signal.

**Table 2: COM_EN Option Header**

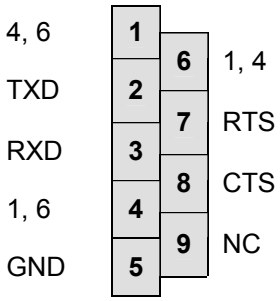
| | | | Shunt | |
|---|---|---|---|---|
| | | | **ON** | **OFF** |
| ▪ | ▪ | CTS | Enabled | Disabled |
| ▪ | ▪ | RTS | Enabled | Disabled |

| | | | | |
|---|---|---|---|---|
| ▪ | ▪ | RXD | Enabled | Disabled |
| ▪ | ▪ | TXD | Enabled | Disabled |

## COM Connector

A standard 9-pin D-sub connector provides external connections for the SCI0 port. The D-sub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The DB9 connector pin-out is shown below.

**Figure 6: COM Connector**




Female DB9 connector that interfaces to the ColdFire internal SCI1 serial port via the U2 RS232 transceiver.

**Pins 1, 4, and 6 are connected together.**

## *SPI Port*

SPI signaling connects directly between connector J1 and the MCU. Refer to the MC52233 Device User Guide available at www.freescale.com for details on using the SPI interface.

## *IIC Port*

IIC signaling connects directly between connector J1 and the MCU. Refer to the MC52233 Device User Guide available at www.freescale.com for details on using the IIC interface.

## *Ethernet*

The AP52233SLK supports ethernet physical-layer communications through an RJ-45 connector at J2. This interface is compatible with IEEE 802.3 at 10/100 Mbps. This port is connected to the Ethernet Physical Layer Transceiver (ePHY) and Fast Ethernet Controller (FEC) internal to the MCU. The coupling transformer T1 provides port isolation. Refer to the MCF52235 documentation at www.freescale.com for further details on operation of the ePHY and FEC. Five LED's provide ethernet port status. These active-low status LED's are driven directly by the MCU.

**Table 3: Ethernet Port Status LED's**

| INDICATOR | COLOR | MCU_SIGNAL | ePHY STATUS |
|---|---|---|---|
| COL | Red | LED_COL | ON – Packet Collision Detected |
| DUP | Green | LED_DUP | ON – Full Duplex, OFF – Half Duplex |
| SPD | Green | LED_SPD | ON – 100T, OFF – 10T |
| LNK | Green | LED_LINK | ON – Link Detected |

| | | | |
|---|---|---|---|
| ACT | Green | LED_ACT | ON – Link Active, TX or RX |

**NOTE:** The Ethernet port must be initialized and active for status indications.

### *Accelerometer*

The AP52233SLK applies an MMA7260Q, 3-axis accelerometer for tilt and motion-sense applications. The accelerometer supports 4 user selectable sensitivities - 1.5g / 2g / 4g / 6g. Separate (X/Y/Z) axis readings are routed to the MCU through the ACC_EN option header. A SLEEP* input allows the device to be placed in a low-power mode.

An option header at ACC_EN allows the user to disconnect the accelerometer if necessary. In default configurations, this option header is not installed and a cut-traces located on the bottom of the board provide a signal path. To disconnect the accelerometer, simply open the cut-trace and install a 1x3 pin-header at ACC_EN. Install a shunt on each signal to reconnect the accelerometer. Table 4 below shows the signal connections to the MCU.

**Table 4: ACC_EN Option Header**

| SIGNAL | MCU INPUT | In default configuration, this option header is not installed. Cut-traces on the bottom of the PCB provide signal pathways. To isolate these analog inputs, simply open the cut-traces and install a 2x3, 0.1" pin header. |
|---|---|---|
| X | AN4 | |
| Y | AN5 | |
| Z | AN6 | |

## *USER OPTIONS*

The AP52233SLK includes various input and output devices to aid application development. User I/O devices include 12 pushbutton switches, 4 green LEDs, and 1 potentiometer. The table below summarizes user option connections on the development board.

**Table 5: User Option Connections**

| OPTION | MCU_PORT | MCU_PIN |
|---|---|---|
| SW1 | IRQ4 | 57 |
| SW2 | IRQ7 | 58 |
| LED1 | DTIN0 | 22 |
| LED2 | DTIN1 | 23 |
| LED3 | DTIN2 | 18 |
| LED4 | DTIN3 | 19 |
| RV1 | AN0 | 25 |

### *Pushbutton Switches*

Two push button switches provide momentary, active-low input, for user applications. Pull-ups internal to the MCU must be enabled to provide error free switch operation. Pushbutton switches SW1 and SW2 are connected to MCU I/O ports IRQ4* and IRQ7* respectively.

## *User LED Indicators*

Four green LED's are provided for use in application development and debug. Each LED is configured active-high. Indicators LED1 through LED4 are enabled by the LED_EN option header. A 3S buffer between the MCU port and the user LED's provides the drive current necessary to control the LED's.

**ON** User LED's enabled active-high

LED_EN

**OFF** User LED's disabled

LED_EN

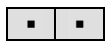
**Figure 7: LED_EN Option Header**

## *Potentiometer*

A 5k ohm, thumb-wheel type, potentiometer at RV1 provides variable resistance input for user applications. The output is the result of a voltage divider that changes as the thumb-wheel is turned. The potentiometer is connected between VDD and GND with the center tap providing the divider output. This center tap is connected to the MCU on signal AN0. The potentiometer may be disconnected from AN0 by means of the POT_EN option header.

**ON** User POT enabled

POT_EN



**OFF** User POT disabled

POT_EN

**Figure 8: POT_EN Option Header**

## I/O PORT CONNECTOR

Connector J1 provides access to the AP52233SLK I/O signals. Signal positions not shown listed are not connected on the board.

| | | | |
|---|---|---|---|
| VDD | **1** | **2** | IRQ4* |
| VSS | **3** | **4** | RSTI* |
| UTXD1 | **5** | **6** | RSTO* |
| URXD1 | **7** | **8** | NC |
| URTS1* | **9** | **10** | ANO |
| UCTS1* | **11** | **12** | AN1 |
| GPT0 | **13** | **14** | AN2 |
| GPT1 | **15** | **16** | AN3 |
| QSPI_DOUT | **17** | **18** | AN4 |
| QSPI_DIN | **19** | **20** | AN5 |
| QSPI_SCLK | **21** | **22** | AN6 |
| QSPO_CS0 | **23** | **24** | AN7 |
| UTXD0 | **25** | **26** | SCL |
| TRXD0 | **27** | **28** | SDA |
| URTS0* | **29** | **30** | GPT2 |
| UCTS0* | **31** | **32** | GPT3 |
| IRQ1* | **33** | **34** | TIN0 |
| SYNCA | **35** | **36** | TIN1 |
| SYNCB | **37** | **38** | TIN2 |
| IRQ7* | **39** | **40** | TIN3 |

**Figure 9: MCU I/O Port Connector**

## OPERATING MODES

The AP52233SLK board operates in two basic modes Run Mode, or Debug Mode.

Run Mode executes user application code from Power-On or Reset, if the RESET vector is programmed.

Debug Mode supports the development and debug of applications via the integrated USB BDM. An optional BDM_PORT is provided but not installed.

See the related sections below for quickly starting the board in the desired mode of operation. The board has been preloaded with a USB stack and open-source RTOS. Refer to the GETTING STARTED section of this document for further details.

### RUN Mode

Run mode executes the user application out of FLASH when power is applied to the board or the RESET button is pressed. Of course, the RESET vector must be programmed to allow application code to execute. Use the following settings to configure the AP52233SLK for RUN Mode using the USB bus to power the board. See the POWER section below for details

1. Connect a serial cable and Ethernet cable between the board and a host PC if required.

2. Connect auxiliary equipment to board if needed.

3. Configure the board option jumpers as shown.

**Table 6: Run Mode Setup**

| | |
|---|---|
| PWR_SEL | Set to VB |
| BDM_EN | OFF |
| COM_EN | ALL ON (if required) |
| VX_EN | ON (if required) |
| LED_EN | ON (if required) |

4. Connect the USB cable to an open USB port on the host PC and attach to the USB port on the target board. LED's D301 and D302 located adjacent to the USB connector, and the VDD LED will light and the loaded application will begin to execute, if the RESET vector has been programmed

## *Debug Mode*

Debug Mode supports application development and debug using the ColdFire background debug module (BDM). Background mode is accessible using either the integrated USB-BDM or an external ColdFire BDM cable. Using the integrated BDM requires a host PC with an available USB port and an A/B USB cable and appropriate hosting software. The USB cable must be USB 2.0 compliant. An external BDM cable can be attached to the 26-pin BDM_PORT header. However, this header is not installed in default configurations. The steps below describe using the integrated USB-BDM. See the POWER section below for details on configuring the board for alternate power input. Connect a serial cable (not included) between the board and a host PC if needed.

1. Connect a serial cable and ethernet cable between the board and a host PC if required.

2. Connect auxiliary equipment to board if required.

3. Install and launch CodeWarrior 6.1 Special Edition, or other software capable of communicating with the ColdFire MCU.

4. Configure the board option jumpers as shown.

**Table 7: Debug Mode Setup**

| | |
|---|---|
| PWR_SEL | Set to VB |
| BDM_EN | ON |
| COM_EN | ALL ON (if required) |
| VX_EN | ON (If required) |
| LED_EN | ON (if required ) |

5. Connect the supplied USB cable between an available USB port on the host PC and the USB connector on the board. LED's D301 and D302 located adjacent to the USB connector, and the VDD LED will light. Hosting development software will establish background communication.

# DEVELOPMENT SUPPORT

Application development and debug for the target MCF52233 is supported through the BDM interface. The debug interface consists of an optional 26-pin header (BDM_PORT) and an integrated USB-BDM debugger. The BDM_PORT header is not installed in default configuration but may be installed by the user if needed. Refer to the MCF52235 Integrated Microcontroller Reference Manual for details on using the Background Debug Module.

Optional JTAG access is also supported through the BDM_PORT header. To use this optional JTAG access, open the cut-trace between pin 1 and pin 2 of the BDM_SEL option header. Install a standard 1x3 header at location BDM_SEL and install a shunt between pin 2 and pin.

Refer to the MCF52235 Integrated Microcontroller Reference Manual (www.freescale.com) for details on using the JTAG port access.

# *SOFTWARE DEVELOPMENT*

Software development requires using a ColdFire assembler or compiler and a host PC running a ColdFire BDM interface. CodeWarrior Special Edition, supplied with this board, allows the user to develop and debug application code and to program flash.

One method to ensure successful application development is to load and execute the application from internal RAM. After the application has been completely debugged, and is fully functional, it can be ported to FLASH. When programmed into FLASH, the application will execute from Power-On or RESET if the RESET vector is programmed.

## *MEMORY MAP*

Refer to the MCF52235 Integrated Microcontroller Reference Manual for details. The latest version can be downloaded from the Freescale web site at www.freescale.com

## *Integrated BDM_PORT*

The AP52233SLK board features an integrated USB-BDM debugger. The integrated debugger supports application development and debugging via the background debug mode. A type B, USB connector provides connectivity between the target board to the host PC.

> **NOTE:** Using the integrated USB BDM requires CodeWarrior 6.1 Special Edition or development tools from P&E Microcomputer Systems.

The integrated debugger provides power and ground to the target, thereby eliminating the need to power the board externally. Power from the integrated USB-BDM is derived from the USB bus and total current consumption is limited by the USB specification. Total current consumption for the target board, and all connected circuitry, must not exceed **500mA**.

Excessive current drain will violate the USB specification causing the bus to disconnect. This will force a target POR.

> **CAUTION:** Violating the USB specification will cause the USB bus to disconnect forcing the target to reset.

## *BDM_PORT Header*

A ColdFire BDM cable may be attached to the 26-pin BDM_PORT port header. This header is not installed in default configuration. Its use requires installing a 2x13, 0.1” center, pin-header. Refer to the BDM documentation, in the device reference manual, for details on using the BDM cable. The BDM_PORT header pin-out is shown below.

Figure 10: BDM Port

| | | | |
|---|---|---|---|
| NC | 1 | 2 | BKPT* |
| GND | 3 | 4 | DSCLK |
| GND | 5 | 6 | TCLK (JTAG) |
| RSTI* | 7 | 8 | DSI |
| VDD | 9 | 10 | DSO |
| GND | 11 | 12 | ALLPST |
| ALLPST | 13 | 14 | ALLPST |
| ALLPST | 15 | 16 | NC |
| NC | 17 | 18 | NC |
| NC | 19 | 20 | GND |
| NC | 21 | 22 | NC |
| GND | 23 | 24 | TCLK (BDM) |
| VDD | 25 | 26 | TA* |

Refer to the MCF52233 Integrated Microcontroller Reference Manual for details on using the BDM_PORT

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