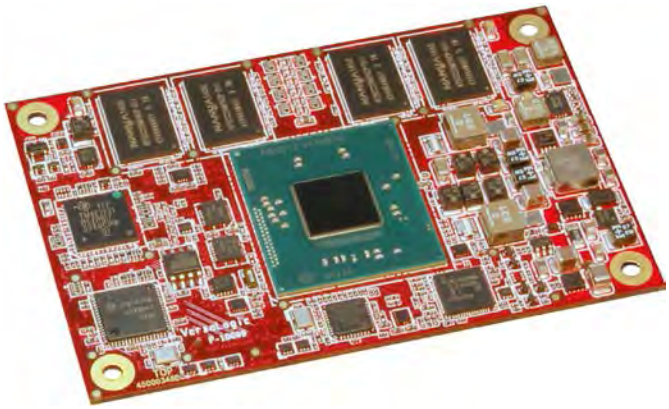
Reference Manual

DOC. REV. 10/15/2015



VL-COMm-33

Intel® Atom™ E38xx-based Computer on Module with SATA, Gigabit Ethernet, USB, Serial, Video, I²C, HD Audio, and PCI Express

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VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

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Product Revision Notes

Revision 1.00	Commercial release

Technical Support

The VL-COMm-33 support page contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Datasheets and manufacturers' links for chips used in this product
- BIOS information and upgrades

This is a private page for VL-COMm-33 users that can be accessed only by entering this address directly. It cannot be reached from the public VersaLogic website.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

Related Products

- Hawk (VL-EPU-3310) VersaLogic baseboard with VL-COMm-33 CPU board.

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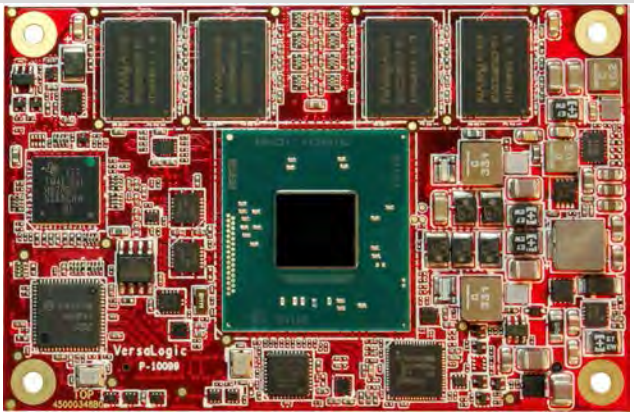
Description



COMm33_10

Figure 1. The VL-COMm-33

HIGHLIGHTS

COM Express Mini Form Factor Extremely small 55 mm x 84 mm format with Type 10 pin-out.	**High-performance Video** Integrated Intel Gen 7 graphics core supports DirectX 11, OpenGL 4.0, and H.264, MPEG-2 encoding/decoding. LVDS video output.
Intel Atom "Bay Trail" Processor Up to 1.9 GHz clock rate. Quad-, dual- or single-core options. Low power consumption.	**Network** Gigabit Ethernet (GbE) with remote boot support.
Industrial Temperature Operation -40° to +85 °C operation for harsh environments.	**RAM** Up to 4 GB soldered-down DDR3L RAM.
MIL-STD-202G Qualified for high shock / vibration environments.	**I/O Interfaces** SATA, PCIe, USB 3.0, USB 2.0, GPIO, serial, HD audio, LPC, SMBus SPI, and I2C.
Fanless Operation No moving parts required for CPU cooling.	**Flash Memory** Up to 8 GB of on-board eMMC flash storage.
Wide Input Voltage Range Accepts 4.75 to 20 volts	**OS Compatibility** Windows 8/7/XP, Windows Embedded Std. 7/XPe/CE, Linux, VxWorks, QNX, DOS

VL-COMm-33 boards are subjected to 100% functional testing and are backed by a limited five-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional COM board.

Technical Specifications

Table 1: Technical Specifications

General	
Form Factor	COM Express mini (Type 10): 55 mm x 84 mm (2.17" x 3.31")
Processor	Intel Atom E38xx platform. 512K 8-way L2 cache per core. Intel 64-bit instructions, Virtualization Technology (VT), and new AES instructions.
Power Requirements @ +12 V (Note 1)	<table><tr><th>Model</th><th>Idle</th><th>Typical</th><th>Maximum</th><th>S3</th></tr><tr><td>VL-COMm-33EAP</td><td>2.5 W</td><td>3.5 W</td><td>4.5 W</td><td>0.4 W</td></tr><tr><td>VL-COMm-33EBP</td><td>3.5 W</td><td>5.6 W</td><td>8.0 W</td><td>0.4 W</td></tr><tr><td>VL-COMm-33EDP</td><td>3.5 W</td><td>7.3 W</td><td>11.0 W</td><td>0.4 W</td></tr></table>
Input Voltage	4.75 V – 20 V (nominal + 5 V or +12 V operation)
System Reset and Hardware Monitors	All voltage rails monitored. Watchdog timer with programmable timeout (1 µs to 10 minutes).
Manufacturing Standards	IPC-A-610 Class 2
Regulatory Compliance	RoHS (2002/95/CE)
Weight	• 31 g – CPU • 63 g – CPU with heat plate • 124 g – CPU with heat plate and heat sink
Environmental	
Operating Temperature	-40 °C to +85 °C. Derate -1.1 °C per 305m (1,000 ft.) above 2,300m (7,500 ft.) ¤ CPU die must be kept below 90 °C
Storage Temperature	-40 °C to +85 °C.
Cooling	Thermal solution required. VersaLogic offers optional heat plate, heat sink, fan, and heat pipe adapter.
Temperature Range and Airflow Requirements	With appropriate thermal solution, maximum temperatures are -40°C to +85°C. Thermal solution at the CPU must be kept below 90 °C • Temperature range: -40 to +85 °C • Airflow: Zero airflow
Altitude	• Operating: To 4,570 m (15,000 ft.) • Storage: To 12,000 m (40,000 ft.)
Thermal Shock	5 °C/min. over operating temperature
Humidity	Less than 95%, noncondensing
Vibration, Sinusoidal Sweep (Note 2)	MIL-STD-202G, Method 204, Modified Condition A: 2g constant acceleration from 5 to 500 Hz, 20 min. per axis
Vibration, Random (Note 2)	MIL-STD-202G, Method 214A, Condition A: 5.35g rms, 5 min. per axis
Mechanical Shock (Note 2)	MIL-STD-202G, Method 213B, Condition G: 20g half-sine, 11 ms duration per axis
Video	
General	Integrated high-performance video. Intel Gen-7 graphics core with 4 Execution Units and Turbo Boost. Supports DirectX 11, OpenGL 4.0, VP8, MPEG2, H.264, and VC1.
VRAM	Up to 224 MB shared DRAM
Desktop Display Interface (Note 3)	1x DDI (Digital Display Interface) with support for • 1x DisplayPort 1.1. Multiplexed with HDMI/DVI ports. Supports Hot-Plug detect • 1x HDMI 1.4 port. Multiplexed with DisplayPort (DP)/DVI. Supports Hot-Plug detect • 1x DVI port. Multiplexed with HDMI/DP ports. Supports Hot-Plug detect
OEM Flat Panel Interface (Note 3)	Single-channel LVDS interface. 18/24-bit. Up to 1920 x 1200 (60 Hz).

Memory	
System RAM	• VL-COMm-33EAP: 2 GB soldered-on DDR3L SDRAM, 1333 MT/s • VL-COMm-33EBP: 2 GB soldered-on DDR3L SDRAM, 1333 MT/s • VL-COMm-33EDP: 4GB soldered-on DDR3L SDRAM, 1333 MT/s
Mass Storage	
Rotating Drives / Flash / SSD (Note 4)	• Two SATA 3 Gb/s ports **(Note 3)** • Optional onboard eMMC 4.5 Flash memory: ▪ VL-COMm-33-EAP: none ▪ VL-COMm-33-EBP: 4 GB ▪ VL-COMm-33-EDP: 8 GB
Network Interface	
Ethernet (Note 1, Note 4)	One auto-detect 10BaseT/100BaseTX/1000BaseT port. Network boot option.
Device I/O	
USB 3.0 (Note 3, Note 5)	One host port
USB 2.0 (Note 3, Note 5)	Seven host ports
COM 1 / 2 (Note 3)	Two-wire, CMOS levels. 16C550 compatible. 3 Gbps max.
GPIO (Note 3)	4 lines multiplexed with the SD card interface
Audio (Note 3)	High Definition Audio (HDA)/digital audio interface with support for multiple codecs.
PCIe (Note 3)	Up to four x1 PCIe (Gen 2) lanes
SMBus (Note 3)	1 MHz
LPC (Note 3)	33 MHz
SPI (Note 3)	Support alternative interface for the BIOS flash device.
I^2C (Note 3)	Fast mode multi-master I²C Bus
Control (Note 3)	Wake, reset, and power
Software	
BIOS	AMI Aptio UEFI BIOS with OEM enhancements. Field reprogrammable.
Sleep Mode	ACPI 3.0. Support for S3 suspend state.
Operating Systems	Compatible with most x86 operating systems including Windows, Windows Embedded, Linux, and VxWorks

Notes:

1. Represents operation at +25 °C with +12 V supply running Windows XP with LVDS display, SATA, GbE, COM, and USB keyboard/mouse. Typical power computed as the mean value of Idle and maximum power specifications. Maximum power measured with 95% CPU utilization.
2. MIL-STD-202G shock and vibe levels are used to illustrate the extreme ruggedness of this product in general. Testing to higher levels and/or different types of shock or vibration methods can be accommodated per the specific requirements of the application. Contact a VersaLogic Sales Engineer for further information.
3. Available via Type 10 I/O connector
4. IEEE 1588 Precision Time Protocol (PTP) compatible
5. Bootable storage device

Specifications are subject to change without notification.

Block Diagram

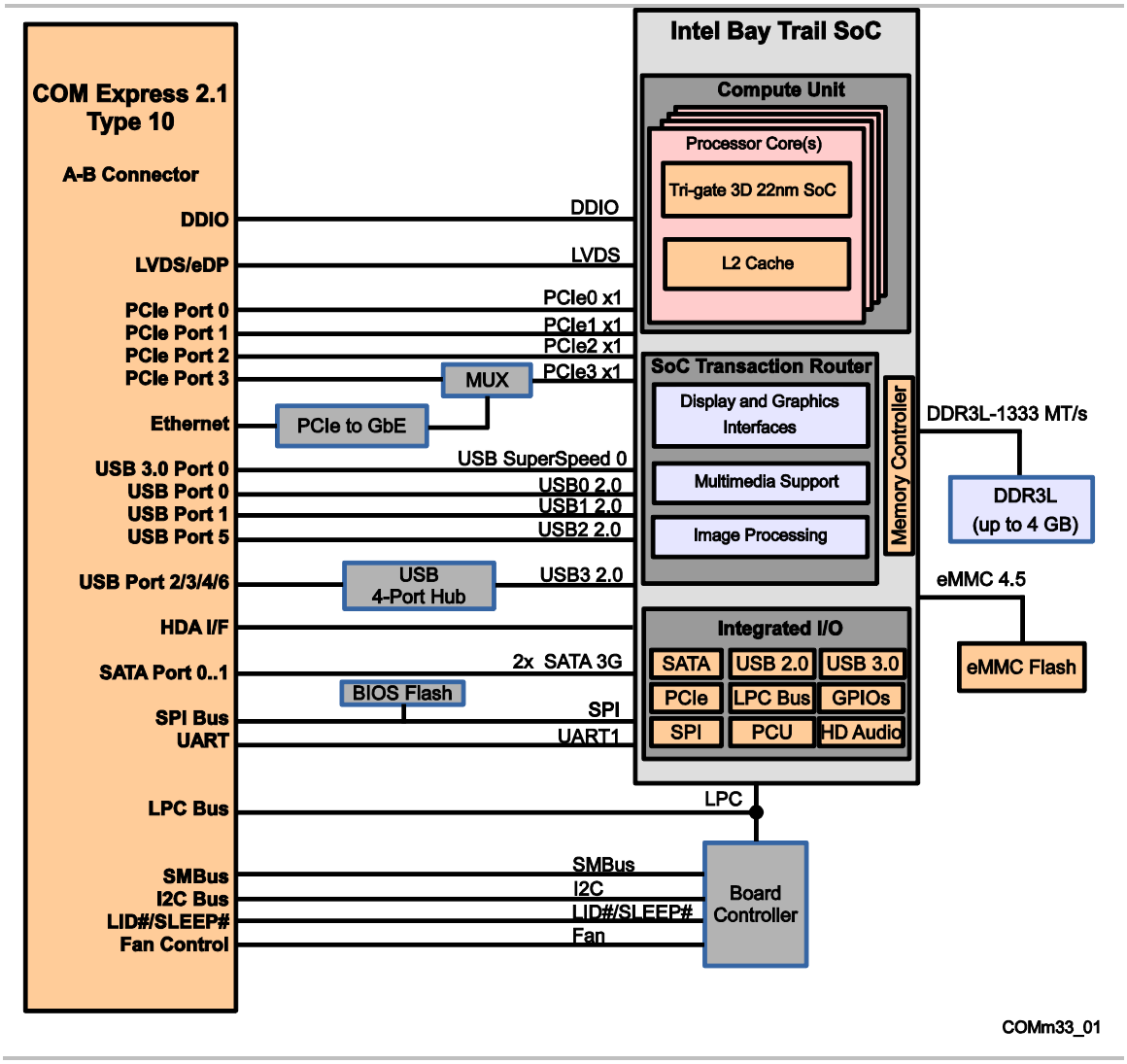


Figure 2. VL-COMm-33 Block Diagram

RoHS Compliance

The VL-COMm-33 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corp. is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Cautions

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

HANDLING CARE

Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

Thermal Considerations

CPU Die Temperature

The CPU die temperature is affected by numerous conditions, such as CPU utilization, CPU speed, ambient air temperature, airflow, thermal effects of adjacent circuit boards, external heat sources, and many others.

The thermal management for the Intel Atom E38xx series of processors consists of a sensor located in the core processor area. The processor contains multiple techniques to help better manage thermal attributes of the processor. It implements thermal-based clock throttling and thermal-based speed step transitions. There is one thermal sensor on the processor and this is used for triggering Intel's thermal monitor. The temperature at which the thermal sensor triggers the thermal monitor is set during the fabrication of the processor. Triggering of this sensor is visible to software by means of the thermal interrupt LVT entry in the local APIC. (See the Intel Atom Processor Series Datasheet for complete information.)

Technical Support

If you are unable to solve a problem after reading this manual, visit the VL-COMm-33 product support web page. The support page provides links to component datasheets, device drivers, and BIOS and PLD code updates.

The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-COMm-33.

If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

Repair Service

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All approved non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. Specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Mark the RMA number clearly on the outside of the box before returning.

Basic Setup

When setting up the VL-COMm-33 in a development environment, it should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the VL-COMm-33 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the VL-COMm-33, including the baseboard and all interface and power cables.

HARDWARE ASSEMBLY

The VL-COMm-33 uses the COM Express Type 10 connector to attach to a baseboard. Attach the VL-COMm-33 to the baseboard as shown in Figure 3.

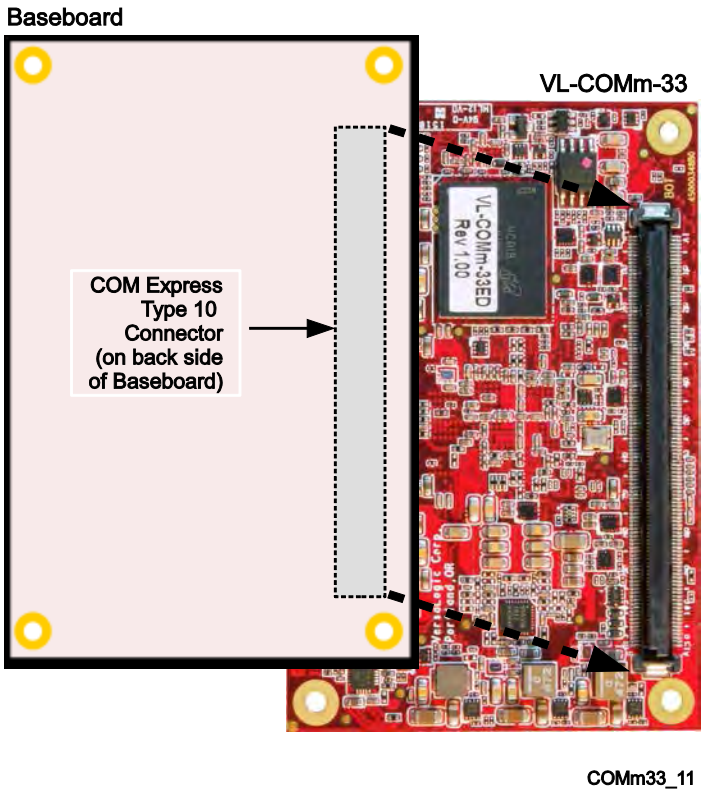


Figure 3. Attaching the VL-COMm-33 to the Baseboard

The hardware used to attach the VL-COMm-33 to the baseboard will depend on the assembly configuration. There are two basic assembly methods:

- Heat plate down (in relation to the enclosure)
- Heat plate up

These assembly methods are shown in Figure 4 and Figure 5, respectively. An optional mounting plate, VL-HDW-405, can be used with either method. See Appendix A – Mounting Options beginning on page 35 for mounting configuration details.

Heat Plate Down

Figure 4 shows the assembly including the mounting plate. Use this assembly method if you are attaching the VL-COMm-33 and baseboard to a larger thermal solution such as a metal chassis/enclosure.

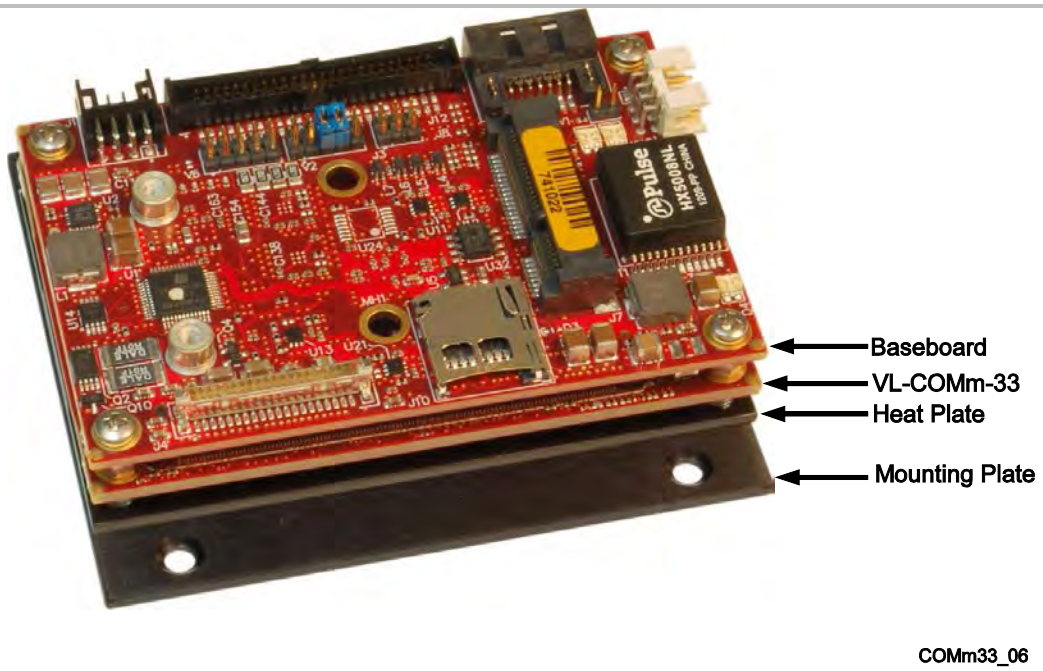


Figure 4. Hardware Assembly with Heat Plate Down

The recommended method is to attach the heat plate (VL-HDW-410) to the mounting plate (VL-HDW-405), and attach the mounting plate to the enclosure.

A thermal interface compound must be applied to the heat plate to thermally bond it to the mounting plate or other surface to which the VL-COMm-33 is mounted. Spread the compound thinly and evenly across the entire heat plate surface before mounting. The Arctic compound is sold separately as part number VL-HDW-401.

Instructions for attaching the heat plate can be found in the section titled “Attaching the Heat Plate to the VL-COMm-33”, beginning on page 38.

Heat Plate Up

Use this assembly method if you are adding a heatsink to the heat plate. Figure 5 shows the assembly including the optional HDW-405 mounting plate and optional HDW-406 heatsink.

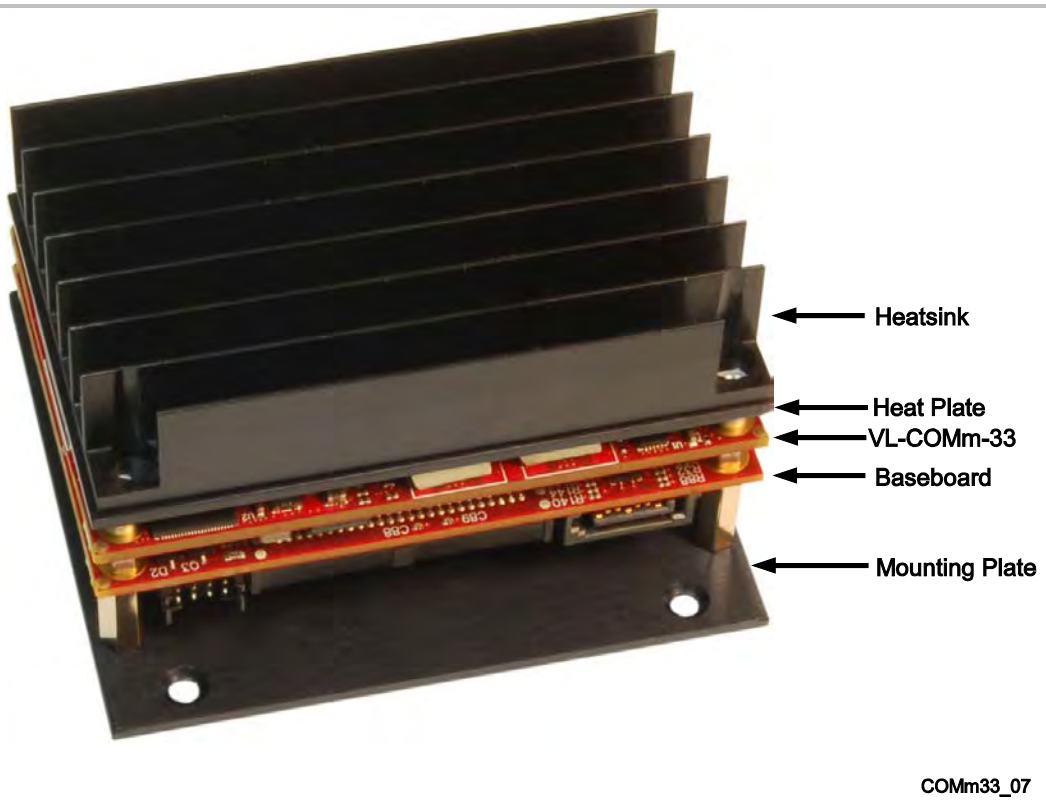


Figure 5. Hardware Assembly with Heat Plate Up

The recommended assembly method for this configuration is as follows:

1. Attach the heatsink to the heat plate.
2. Attach the baseboard to the mounting plate (VL-HDW-405) with standoffs.
3. Attach the mounting plate to the enclosure.

BIOS Setup

Refer to the VersaLogic System Utility Reference Manual for information on how to configure the VL-COMm-33 BIOS.

Operating System Installation

The standard PC architecture used on the VL-COMm-33 makes the installation and use of most of the standard x86-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular OS, or a link to the drivers, are available at the VL-COMm-33 Product Support web page.

Dimensions and Mounting

VL-COMm-33 Dimensions

The VL-COMm-33 complies with COM Express Mini form factor standards.

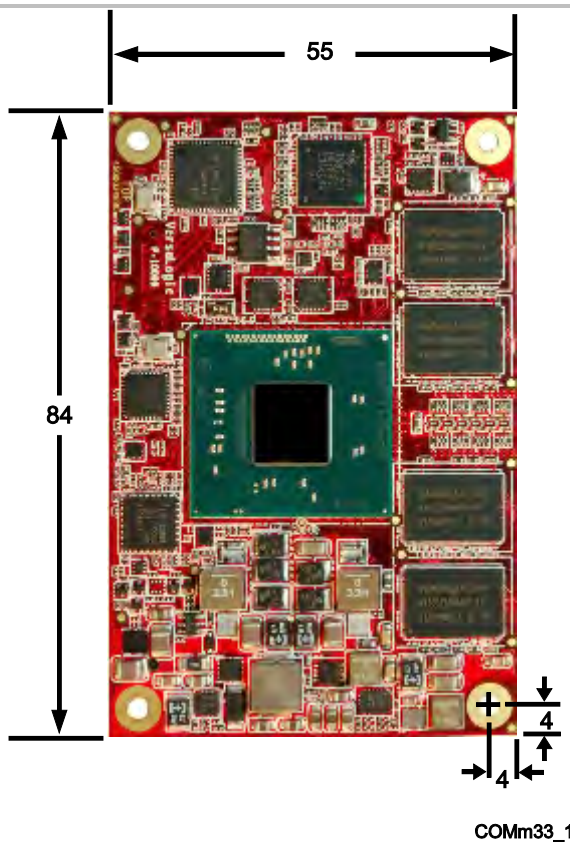


Figure 6. VL-COMm-33 Dimensions and Mounting Holes
(Not to scale. All dimensions in millimeters.)

COM Express Type 10 Connector

- Figure 7 shows the location of the COM Express Type 10 connector.
- Table 4 (beginning on page 23) lists the pin-out for the COM Express Type 10 connector.
- A compatible mating connector is Tyco 3-1827253-6.

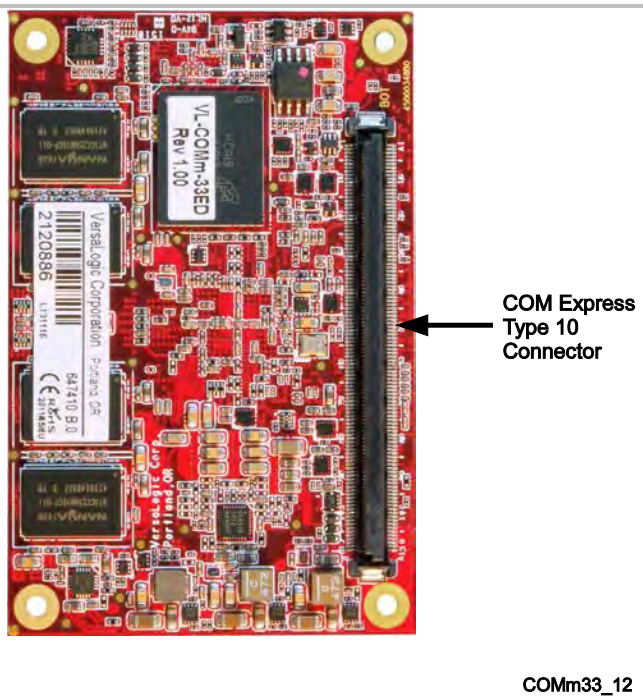


Figure 7. Location of COM Express Type 10 Connector

VL-HDW-405 Mounting Plate Dimensions

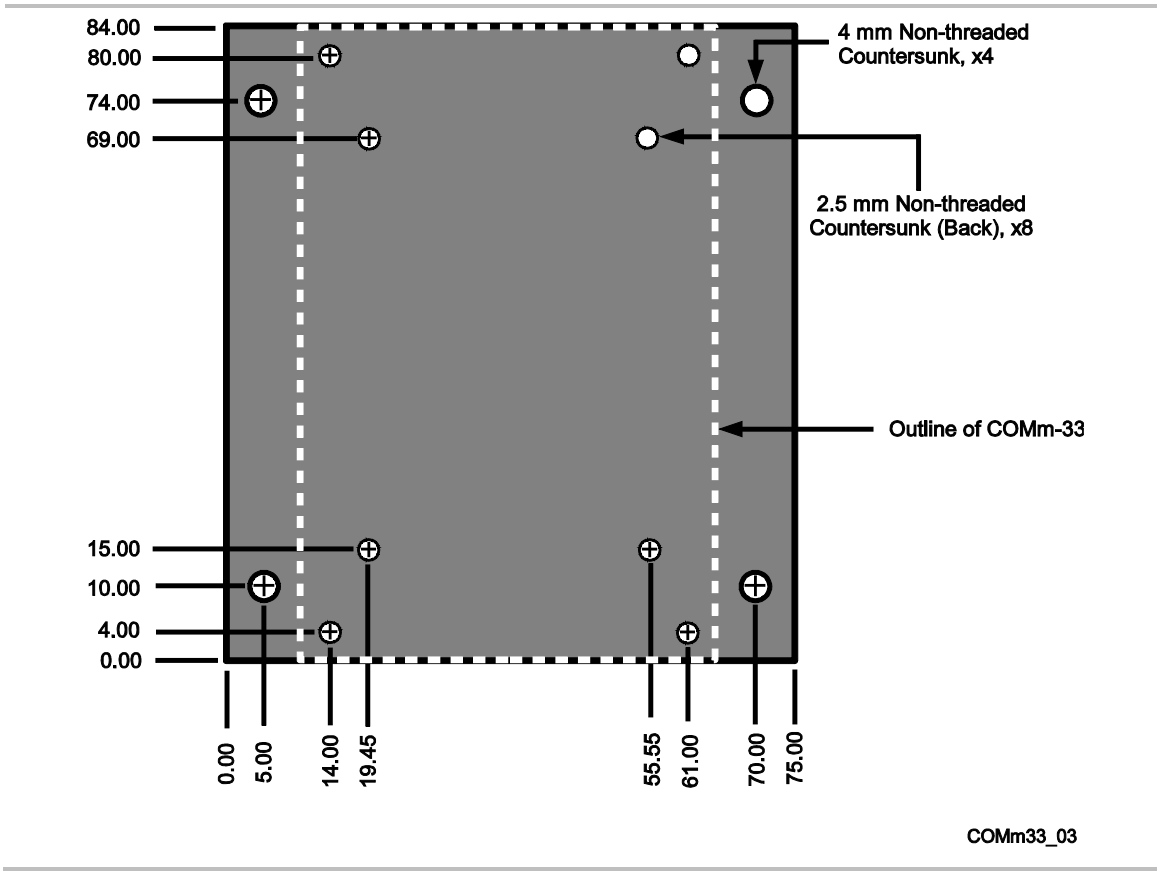


Figure 8. Mounting Plate Dimensions
(Not to scale. All dimensions in millimeters.)

Power Supply

Main power is applied to the VL-COMm-33 through the COM Express Type 10 connector. All 12V pins on the Type 10 connector should be connected to the input payload power supply.

POWER REQUIREMENTS

The VL-COMm-33 requires a single +4.75 – 20 VDC supply of 2A (24 W) or better. A +5V standby power rail may be supplied to support standby functions and a +3V battery input for applications that require the RTC to keep time in the absence of the main and standby power supplies. The exact power requirements for the VL-COMm-33 depend on several factors, including memory configuration, CPU speed, peripheral connections, and attached devices, etc. For example, driving long RS-232 lines at high speed can increase power demand.

SUPPLY VOLTAGE STANDARD POWER

The VL-COMm-33 has a power input range of 4.75V – 20 V.

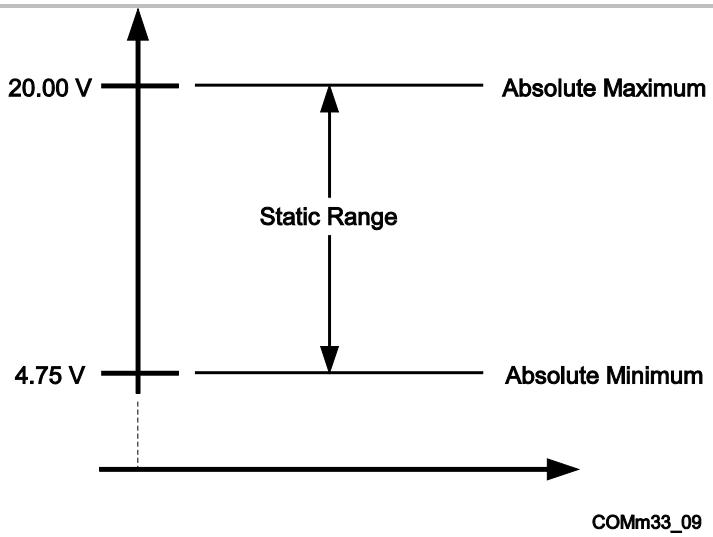


Figure 9. Static Range of Power Input

ELECTRICAL CHARACTERISTICS

Power supply pins on the board's connectors limit the amount of input power. Table 2 provides an overview of the limitations for pinout Type 10 (single connector, 220 pins).

Table 2: Power Limitations for COM Express Type 10 Connector

	Power Rail		
	Wide Input	**VCC_5V-STBY**	**VCC_RTC**
Module Pin Current Capability (Amps)	6	2	0.5
Nominal Input (Volts)	---	5	3
Input Range (Volts)	4.75 – 20.00	4.75 – 5.25	2.0 – 3.3
De-rated Input (Volts)	4.75	4.75	---
Maximum Input Ripple (10 Hz to 20 MHz) (mV)	±100	±50	±20
Maximum Module Input Power (de-rated input) (Watts)	28	9	---
Assumed Conversion Efficiency	85%	---	---
Maximum Load Power (Watts)	23.8	---	---

RISE TIME

The input voltages shall rise from 10% of nominal to 95% of nominal within 0.1 ms to 20 ms (0.1 ms ≤ Rise Time ≤ 20 ms). Each DC input voltage must rise from 10% to 90% of its nominal voltage in a smooth, continuous ramp and the slope of the turn-on waveform must be positive.

CPU

The Intel Atom E38xx SoC features integrated 3D graphics, video encode/decode, memory controller, and display controller in one package.

System RAM

The VL-COMm-33 has 4 GB or 2 GB of soldered-on DDR3L-1333 SDRAM.

Real-Time Clock (RTC)

The VL-COMm-33 features a real-time clock/calendar (RTC) circuit. The VL-COMm-33 supplies RTC voltage in S5, S3, and S0 states, but requires an external battery connection to pin A47 of the COM Express Type 10 connector to maintain its functionality and its RAM when the VL-COMm-33 is not powered. The RTC can be set using the BIOS Setup program.

Watchdog Timer

The VL-COMm-33 has a watchdog timer that contains a selectable prescaler approximately 1 µs to 10 minutes. See the Intel Atom Processor Series Datasheet for configuration information.

Default BIOS Settings

The VL-COMm-33 permits you to store user-defined BIOS settings. This enables you to retrieve those settings from cleared or corrupted CMOS RAM, or battery failure. All BIOS defaults can be changed, except the time and date. BIOS defaults can be updated with the BIOS Update Utility.

CAUTION: If BIOS default settings make the system unbootable and prevent the user from entering the BIOS Setup program, the VL-COMm-33 must be serviced by the factory.

DEFAULT BIOS SETUP VALUES

After CMOS RAM is cleared, the system loads default BIOS parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

5 Interfaces and Connectors

Gigabit Ethernet

The VL-COMm-33 offers a Gigabit Ethernet interface on the COM Express connector via the onboard Intel® I210 Gigabit Ethernet controller. This controller is connected to the Intel Bay Trail SoC through the fourth PCI Express lane.

The Ethernet interface consists of four pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3±, plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ-45 connector with integrated or external isolation magnetics on the baseboard.

Gigabit Ethernet signals routed to the COM Express Type 10 connector are described in Table 6 on page 26.

Serial ATA™ (SATA)

Two SATA interfaces are present on the COM Express connector via a SATA host controller integrated in the Intel Bay Trail SoC. The controller supports independent DMA operation and data transfer rates of 1.5 Gb/s and 3.0 Gb/s. It also supports two modes of operation: legacy mode and AHCI mode. Software that uses legacy mode will not have AHCI capabilities.

Serial ATA signals routed to the COM Express Type 10 connector are described in Table 7 on page 27.

PCI Express™

The VL-COMm-33 default offers up to three PCI Express lanes externally on the connector (PCIe 0-2). The default configuration for the lanes on the COM Express connector is 3x1.

The PCI Express interface is based on the PCI Express Specification 2.0 with Gen 1 (2.5 Gb/s) and Gen 2 (5 Gb/s) speed.

PCI Express signals routed to the COM Express Type 10 connector are described in Table 8 on page 27.

High-Definition Audio (HDA) Interface

The VL-COMm-33 provides an interface that supports the connection of HDA audio codecs. Drivers are available for most Windows-based and Linux operating systems. To obtain the most current versions, consult the VL-COMm-33 support page.

High-Definition audio signals routed to the COM Express Type 10 connector are described in Table 5 on page 26.

SD Card Interface

The VL-COMm-33 offers a 4-bit SD interface for SD/MMC cards on the COM Express connector. The SD signals are multiplexed with GPIO signals and controlled by the Board controller device. The SD card controller in the Storage Control Cluster of the SoC supports the SD interface with up to 832 Mb/s data rate using four parallel data lines.

SD Card interface signals routed to the COM Express Type 10 connector are described in Table 24 on page 33.

Serial Ports

The VL-COMm-33 provides two UARTs. Hardware handshaking and hardware flow control are not supported. These asynchronous serial ports are intended for general purpose use and for use with debugging software that makes use of console redirect features available in many operating systems.

Serial port signals routed to the COM Express Type 10 connector are described in Table 17 on page 31

I²C Interface

The I²C bus is implemented through the Board controller device, providing a fast mode multi-master I²C Bus.

I²C bus signals routed to the COM Express Type 10 connector are described in Table 18 on page 31

Universal Serial Bus (USB)

USB signals routed to the COM Express Type 10 connector are described in Table 10 on page 28. For information on how the USB host controllers are routed, refer to the section titled USB Port Mapping on page 20

USB 2.0

The VL-COMm-33 offers seven USB 2.0 interfaces on the COM Express connector:

- Three ports are routed directly from the SoC to the COM Express connector
- Four ports are routed to the COM Express connector through a four-port USB hub.

The EHCI host controller in the SoC supports these interfaces with high-speed, full-speed, and low-speed USB signaling. The controller complies with USB standard 1.1 and 2.0.

Note: Only USB 2.0 port 1 can be used as a debug port.

USB 3.0

The VL-COMm-33 includes one USB 3.0 interface on the COM Express connector. This interface is controlled by an xHCI host controller in the SoC. The host controller allows data transfers of up to 5 Gb/s and supports SuperSpeed, high-speed, full-speed and low-speed USB signaling.

USB PORT MAPPING

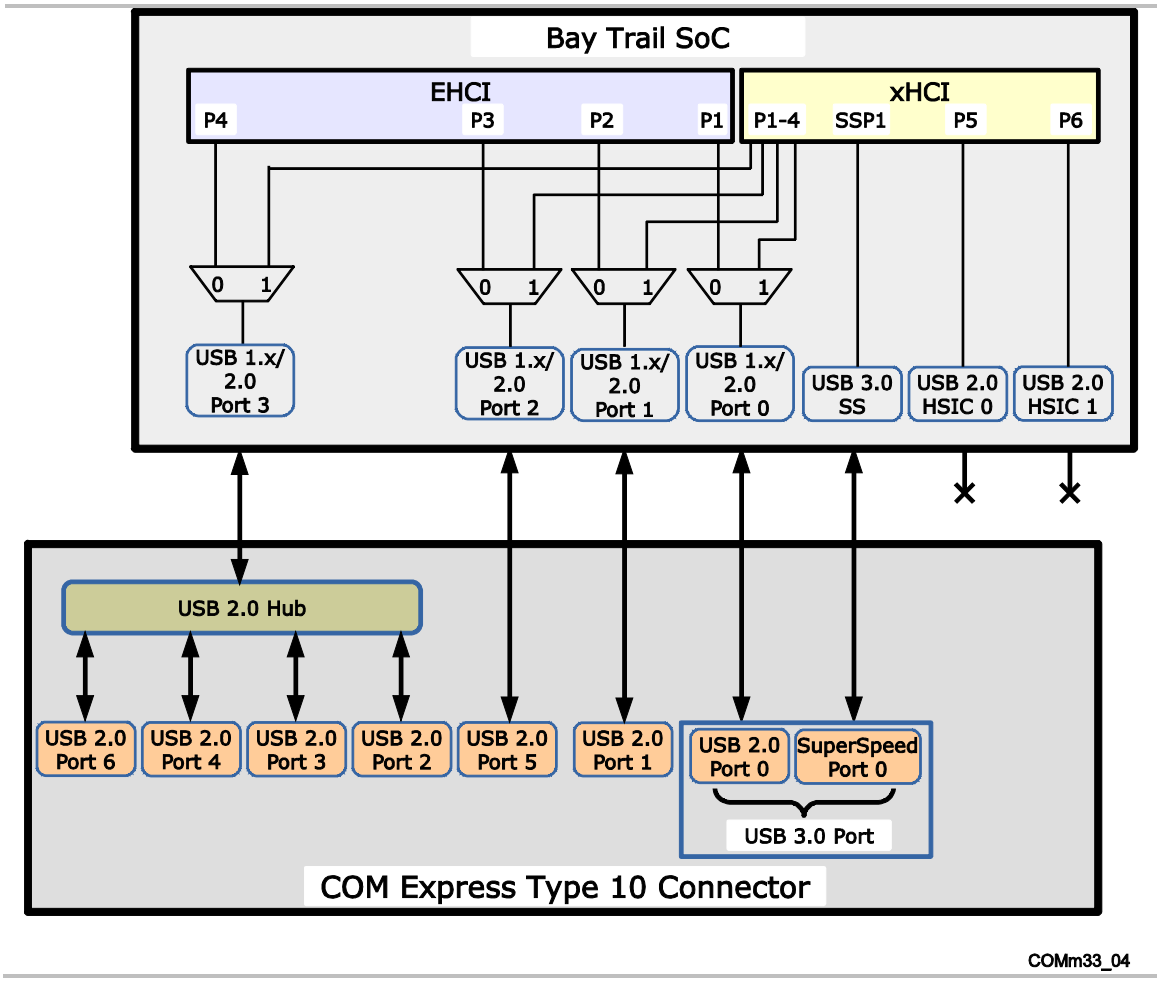


Figure 10. USB Port Mapping

Express Card™

The board supports the implementation of ExpressCards. Such an implementation requires the dedication of one USB port and a x1 PCI Express link for each ExpressCard used.

Express Card signals routed to the COM Express Type 10 connector are described in Table 9 on page 27.

Digital Display Interface

The board includes one Digital Display Interface (DDI0) on the COM Express connector. It also offers an LVDS interface on the second Digital Display Interface (DDI1) by default.

Digital Display Interface signals routed to the COM Express Type 10 connector are described in Table 14 on page 30.

The VL-COMm-33 supports eDP 1.3, DP 1.1a, DVI or HDMI 1.4a, audio on DP and HDMI, High-bandwidth Digital Content Protection 1.4/2.1 and up to two independent displays. Table 3 lists the supported display combinations.

Table 3: Supported Display Combinations

Display 1	Display 2	Display1 maximum resolution	Display2 maximum resolution
DDI (DP, HDMI/DVI)	LVDS/eDP	• 1920x1200 @ 60Hz (HDMI/DVI) • 2560x1600 @ 60Hz (DP)	1400x1050 @ 60 Hz (single channel LVDS)
LVDS/eDP	DDI (DP, HDMI/DVI)	1400x1050 @ 60Hz (single channel LVDS)	• 1920x1200 @ 60 Hz (HDMI/DVI) • 2560x1600 @ 60 Hz (DP)

HDMI

The VL-COMm-33 supports one HDMI interface at a maximum resolution of 1920x1200 @ 60 Hz. Refer to Table 3 for possible display combinations.

HDMI signals routed to the COM Express Type 10 connector are described in Table 16 on page 31.

DVI

The VL-COMm-33 supports one DVI interface at a maximum resolution of 1920x1200 @ 60 Hz. Refer to Table 3 for possible display combinations.

DVI signals routed to the COM Express Type 10 connector are described in Table 16 on page 31.

DISPLAY PORT (DP)

The VL-COMm-33 supports one DP interface at a maximum resolution of 2560x1600 @ 60 Hz. Refer to Table 3 for possible display combinations.

Display Port signals routed to the COM Express Type 10 connector are described in Table 15 on page 30.

LVDS Interface

The board offers a 24 bpp single channel LVDS interface on the COM Express connector. The interface is provided by routing the onboard PTN3460 to the SoC's second Digital Display Interface.

The PTN3460 processes incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. It supports the single channel signaling on the VL-COMm-33 with color depths of 18 bits or 24 bits per pixel and a pixel clock frequency up to 112 MHz.

LVDS signals routed to the COM Express Type 10 connector are described in Table 11 on page 29.

LPC Bus

The board includes an LPC (Low Pin Count) bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be implemented on an application specific baseboard using this bus. Only certain devices such as Super I/O or TPM chips can be implemented on the baseboard.

LPC bus signals routed to the COM Express Type 10 connector are described in Table 12 on page 29

SPI Interface

An SPI interface that supports booting from an external SPI flash is available on the VL-COMm-33 via the Intel Bay Trail SoC. The board implements an SPI interface as an alternative interface for the BIOS flash device. An SPI flash device can be used as a replacement for a firmware hub.

SPI interface signals routed to the COM Express Type 10 connector are described in Table 13 on page 30

COM Express™ Type 10 Connector

The 220-pin COM Express connector uses the Type 10 pin-out definition. The default feature set includes three PCI Express lanes, one Gigabit Ethernet port, six USB 2.0 ports, one USB 3.0/2.0 port, two SATA ports, LVDS, SDVO, HDA, two serial ports, watchdog timer, and speaker. Modules implementing Pin-out Type 10 should use the pin-out shown in Table 4.

Table 4: COM Express Connector Pinout

Pin	Row A Signal	Pin	Row B Signal
A1	GND(FIXED)	B1	GND(FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	LPC_DRQ0# (*)
A9	GBE0_MDI1-	B9	LPC_DRQ1# (*)
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND(FIXED)	B11	GND(FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND(FIXED)	B21	GND(FIXED)
A22	USB_SSRX0-	B22	USB_SSTX0-
A23	USB_SSRX0+	B23	USB_SSTX0+
A24	SUS_S5#	B24	PWR_OK
A25	USB_SSRX1-	B25	USB_SSTX1-
A26	USB_SSRX1+	B26	USB_SSTX1+
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0
A31	GND(FIXED)	B31	GND(FIXED)
A32	AC/HDA_BITCLK	B32	SPKR
A33	AC/HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#

Pin	Row A Signal
A36	USB6-
A37	USB6+
A38	USB_6_7_OC#
A39	USB4-
A40	USB4+
A41	GND(FIXED)
A42	USB2-
A43	USB2+
A44	USB_2_3_OC#
A45	USB0-
A46	USB0+
A47	VCC_RTC
A48	EXCD0_PERST#
A49	EXCD0_CPPE#
A50	LPC_SERIRQ
A51	GND(FIXED)
A52	RSVD
A53	RSVD
A54	GPI0
A55	RSVD
A56	RSVD
A57	GND
A58	PCIE_TX3+
A59	PCIE_TX3-
A60	GND(FIXED)
A61	PCIE_TX2+
A62	PCIE_TX2-
A63	GPI1
A64	PCIE_TX1+
A65	PCIE_TX1-
A66	GND
A67	GPI2
A68	PCIE_TX0+
A69	PCIE_TX0-
A70	GND(FIXED)
A71	LVDS_A0+
A72	LVDS_A0-
A73	LVDS_A1+
A74	LVDS_A1-
A75	LVDS_A2+
A76	LVDS_A2-
A77	LVDS_VDD_EN
A78	LVDS_A3+
A79	LVDS_A3-

Pin	Row B Signal
B36	USB7-
B37	USB7+
B38	USB_4_5_OC#
B39	USB5-
B40	USB5+
B41	GND(FIXED)
B42	USB3-
B43	USB3+
B44	USB_0_1_OC#
B45	USB1-
B46	USB1+
B47	EXCD1_PERST#
B48	EXCD1_CPPE#
B49	SYS_RESET#
B50	CB_RESET#
B51	GND(FIXED)
B52	RSVD
B53	RSVD
B54	GPO1
B55	RSVD
B56	RSVD
B57	GPO2
B58	PCIE_RX3+
B59	PCIE_RX3-
B60	GND(FIXED)
B61	PCIE_RX2+
B62	PCIE_RX2-
B63	GPO3
B64	PCIE_RX1+
B65	PCIE_RX1-
B66	WAKE0#
B67	WAKE1#
B68	PCIE_RX0+
B69	PCIE_RX0-
B70	GND(FIXED)
B71	DDI0_PAIR0+
B72	DDI0_PAIR0-
B73	DDI0_PAIR1+
B74	DDI0_PAIR1-
B75	DDI0_PAIR2+
B76	DDI0_PAIR2-
B77	DDI0_PAIR4+
B78	DDI0_PAIR4-
B79	LVDS_BKLT_EN

Pin	Row A Signal
A80	GND(FIXED)
A81	LVDS_A_CK+
A82	LVDS_A_CK-
A83	LVDS_I2C_CK
A84	LVDS_I2C_DAT
A85	GPI3
A86	RSVD
A87	RSVD
A88	PCIE_CLK_REF+
A89	PCIE_CLK_REF-
A90	GND(FIXED)
A91	SPI_POWER
A92	SPI_MISO
A93	GPO0
A94	SPI_CLK
A95	SPI_MOSI
A96	TPM_PP
A97	TYPE10#
A98	SER0_TX
A99	SER0_RX
A100	GND(FIXED)
A101	SER1_TX
A102	SER1_RX
A103	LID#
A104	VCC_12V
A105	VCC_12V
A106	VCC_12V
A107	VCC_12V
A108	VCC_12V
A109	VCC_12V
A110	GND(FIXED)

Pin	Row B Signal
B80	GND(FIXED)
B81	DDI0_PAIR3+
B82	DDI0_PAIR3-
B83	LVDS_BKLT_CTRL
B84	VCC_5V_SBY
B85	VCC_5V_SBY
B86	VCC_5V_SBY
B87	VCC_5V_SBY
B88	BIOS_DIS1#
B89	DD0_HPD
B90	GND(FIXED)
B91	DDI0_PAIR5+
B92	DDI0_PAIR5-
B93	DDI0_PAIR6+
B94	DDI0_PAIR6-
B95	DDI0_DDC_AUX_SEL
B96	RSVD
B97	SPI_CS#
B98	DDI0_CTRLCLK_AUX+
B99	DDI0_CTRLDATA_AUX-
B100	GND(FIXED)
B101	FAN_PWMOUT
B102	FAN_TACHIN
B103	SLEEP#
B104	VCC_12V
B105	VCC_12V
B106	VCC_12V
B107	VCC_12V
B108	VCC_12V
B109	VCC_12V
B110	GND(FIXED)

COM Express Signal Descriptions

Table 5: High Definition Audio Link Signal Descriptions

Signal	COM Express Pin Number	Description
AC/HDA_RST# (Note 1)	A30	**High Definition Audio Reset:** The master hardware reset to external codec(s).
AC/HDA_SYNC (Note 1)	A29	**High Definition Audio Sync:** A 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.
AC/HDA_BITCLK (Note 1)	A32	**High Definition Audio Bit Clock Output:** A 24.000 MHz serial data clock generated by the Intel High Definition Audio controller.
AC/HDA_SDOUT (Note 1)	A33	**High Definition Audio Serial Data Out:** The serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio.
AC/HDA_SDIN[2:0] (Note 1, Note 2)	B28-B30	**High Definition Audio Serial Data In [0]:** Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel High Definition Audio.

Notes:
1. AC'97 codecs are not supported.
2. HDA_SDIN[2:1] are not connected.

Table 6: Gigabit Ethernet Signal Descriptions

Signal	COM Express Pin Number	Description
GBE0_MDI0+	A13	Gigabit Ethernet Controller 0: Media Dependent Interface differential pairs 0, 1, 2, 3 for an external transformer. The MDI can operate in 1000, 100, and 10 Mbit/sec modes. Some pairs are unused in some modes according to the following:
GBE0_MDI0-	A12	
GBE0_MDI1+	A10	
GBE0_MDI1-	A9	
GBE0_MDI2+	A7	
GBE0_MDI2-	A6	
GBE0_MDI3+	A3	
GBE0_MDI3-	A2	
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK# (Note 1)	A8	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low.
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low.
GBE0_CTREF (Note 2)	A14	Reference voltage for Baseboard Ethernet channel 0 magnetics center tap.

	1000	100	10
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-		
MDI[2]+/-	B1_DC+/-		

Notes:
1. Only active during a 100 Mbit or 1 Gbit connection; it is not active during a 10 Mbit connection.
2. Not connected

Table 7: Serial ATA Signal Descriptions

Signal	COM Express Pin Number	Description	Notes
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0 Receive Input differential pair	Supports Serial ATA specification, Revision 2.6
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0 Transmit Output differential pair	
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1 Receive Input differential pair	
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1 Transmit Output differential pair	

Table 8: PCI Express Signal Descriptions

Signal	COM Express Pin Number	Description
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0 Receive input differential pair.
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0 Transmit output differential pair.
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1 Receive input differential pair.
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1 Transmit output differential pair.
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2 Receive input differential pair.
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2 Transmit output differential pair.
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3 Receive input differential pair.
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3 Transmit output differential pair.
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express reference clock output for all PCI Express lanes. (Note)

Note: A PCI Express Gen2/3 compliant clock buffer chip must be used on the baseboard if more than one PCI Express device is designed in.

Table 9: Express Card Support Signal Descriptions

Signal	COM Express Pin Number	Description
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset

Table 10: USB Signal Descriptions

Signal	COM Express Pin Number	Description	Notes
USB0+ USB0-	A46 A45	USB Port 0 differential data pairs	Note 1
USB1+ USB1-	B46 B45	USB Port 1 differential data pairs	Note 2
USB2+ USB2-	A43 A42	USB Port 2 differential data pairs	Note 3
USB3+ USB3-	B43 B42	USB Port 3 differential data pairs	Note 3
USB4+ USB4-	A40 A39	USB Port 4 differential data pairs	Note 3
USB5+ USB5-	B40 B39	USB Port 5 differential data pairs	Note 4
USB6+ USB6-	A37 A36	USB Port 6 differential data pairs	Note 3
USB7+ USB7-	B37 B36	USB Port 7 differential data pairs	Note 5
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the baseboard may drive this line low.	Note 6
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the baseboard may drive this line low.	Note 6
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the baseboard may drive this line low.	Note 6
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the baseboard may drive this line low.	Note 6
USB_SSTX0+ USB_SSTX0-	B23 B22	Additional transmit signal differential pairs for the SuperSpeed USB data path.	---
USB_SSTX1+ USB_SSTX1-	B26 B25	Additional transmit signal differential pairs for the SuperSpeed USB data path.	Note 5
USB_SSRX0+ USB_SSRX0-	A23 A22	Additional receive signal differential pairs for the SuperSpeed USB data path.	---
USB_SSRX1+ USB_SSRX1-	A26 A25	Additional receive signal differential pairs for the SuperSpeed USB data path.	Note 5

Notes:

1. USB 2.0 compliant. Backwards compatible to USB 1.1 Default port to form Native USB 3.0 port.
2. USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB port. Only this port can be used as debug port.
3. USB 2.0 compliant. Backwards compatible to USB 1.1 Routed via on-module USB hub.
4. USB 2.0 compliant. Backwards compatible to USB 1.1 Native USB port.
5. Not connected.
6. Do not pull this line high on the baseboard.

Table 11: LVDS Signal Descriptions

Signal	COM Express Pin Number	Description
LVDS_A0+	A71	LVDS Channel A differential pair 0
LVDS_A0-	A72	LVDS Channel A differential pair 0
LVDS_A1+	A73	LVDS Channel A differential pair 1
LVDS_A1-	A74	LVDS Channel A differential pair 1
LVDS_A2+	A75	LVDS Channel A differential pair 2
LVDS_A2-	A76	LVDS Channel A differential pair 2
LVDS_A3+	A78	LVDS Channel A differential pair 3
LVDS_A3-	A79	LVDS Channel A differential pair 3
LVDS_A_CK+	A81	LVDS Channel A differential clock
LVDS_A_CK-	A82	LVDS Channel A differential clock
LVDS_VDD_EN	A77	Panel power enable
LVDS_BKLT_EN	B79	Panel backlight enable
LVDS_BKLT_CTRL	B83	Panel backlight brightness control
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.

Table 12: LPC Signal Descriptions

Signal	COM Express Pin Number	Description
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed address, command and data bus
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC serial DMA requests (Not connected)
LPC_SERIRQ	A50	LPC serial interrupt
LPC_CLK	B10	LPC clock output

Table 13: SPI Signal Descriptions

Signal	COM Express Pin Number	Description
SPI_CS#	B97	Chip select for baseboard SPI.
SPI_MISO	A92	Master Input Slave Output: SPI output data from baseboard SPI device to module.
SPI_MOSI	A95	Master Output Slave Input: SPI output data from module to baseboard SPI.
SPI_CLK	A94	Clock from module to baseboard SPI BIOS flash.
SPI_POWER	A91	Power source for baseboard SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Ground to select external SPI.

Table 14: DDI Signal Descriptions

Signal	COM Express Pin Number	Description
DDI0_PAIR0+ DDI0_PAIR0-	B71 B72	Digital Display Interface 0 Pair 0 differential pairs (Note)
DDI0_PAIR1+ DDI0_PAIR1-	B73 B74	Digital Display Interface 0 Pair 1 differential pairs (Note)
DDI0_PAIR2+ DDI0_PAIR2-	B75 B76	Digital Display Interface 0 Pair 2 differential pairs (Note)
DDI0_PAIR3+ DDI0_PAIR3-	B81 B82	Digital Display Interface 0 Pair 3 differential pairs (Note)
DDI0_HPD	B89	Digital Display Interface Hot Plug Detect
DDI0_CTRLCLK_AUX+	B98	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect. HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high
DDI0_CTRLDATA_AUX-	B99	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.

Note: Only TMDS/DP option, no SDVO.

Table 15: DisplayPort (DP) Signal Descriptions

Signal	COM Express Pin Number	Description
DP0_LANE0+ DP0_LANE0-	B71 B72	Uni-directional main link for the transport of isochronous streams and secondary data.
DP0_LANE1+ DP0_LANE1-	B73 B74	
DP0_LANE2+ DP0_LANE2-	B75 B76	
DP0_LANE3+ DP0_LANE3-	B81 B82	
DP0_HPD	B89	Detection of hot plug/unplug and notification of the link layer.
DP0_AUX+	B98	Half-duplex bi-directional aux channel for services such as link configuration or maintenance and EDID access.
DP0_AUX-	B99	

Table 16: HDMI/DVI Signal Descriptions

Signal	COM Express Pin Number	Description
TMDS0_DATA2+ TMDS0_DATA2-	B71 B72	HDMI/DVI TMDS lane 2 differential pair.
TMDS0_DATA1+ TMDS0_DATA1-	B73 B74	HDMI/DVI TMDS lane 1 differential pair.
TMDS0_DATA0+ TMDS0_DATA0-	B75 B76	HDMI/DVI TMDS lane 0 differential pair.
TMDS0_CLK + TMDS0_CLK -	B81 B82	HDMI/DVI TMDS Clock output differential pair.
HDMI0_HPD	B89	HDMI/DVI Hot-plug detect.
HDMI0_CTRLCLK	B98	HDMI/DVI I2C Control Clock
HDMI0_CTRLDATA	B99	HDMI/DVI I2C Control Data

Table 17: Serial Interface Signal Descriptions

Signal	COM Express Pin Number	Description
SER0_TX	A98	General purpose serial port transmitter
SER0_RX	A99	General purpose serial port receiver
SER1_TX	A101	General purpose serial port transmitter
SER1_RX	A102	General purpose serial port receiver

Table 18: I^2C Signal Descriptions

Signal	COM Express Pin Number	Description
I2C_CK	B33	General purpose I2C port clock output
I2C_DAT	B34	General purpose I2C port data I/O line

Table 19: Miscellaneous Signal Descriptions

Signal	COM Express Pin Number	Description
SPKR	B32	Output for audio enunciator; the “speaker” in PC-AT systems
WDT	B27	Output indicating that a watchdog time-out event has occurred.
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.
FAN_TACHIN	B102	Fan tachometer input.
TPM_PP	A96	Physical presence pin of Trusted Platform Module (TPM). This feature is not implemented.

Table 20: Power and System Management Signal Descriptions

Signal	COM Express Pin Number	Description
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.
SYS_RESET#	B49	Reset button input. Active low input, edge triggered. System will not be held in hardware reset while this input is kept low.
CB_RESET#	B50	Reset output from module to Baseboard. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a main power input (V_{IN}) that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.
SUS_STAT#	B18	Suspend Status: Indicates the system will enter a low power state soon. Used to notify LPC devices.
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the baseboard may be used to enable the non-standby power on a typical ATX power supply.
SUS_S4#	A18	Indicates system is in Suspend-to-disk (S4) or Soft off (S5) state. Active low output. Same signal as SUS_5#.
SUS_S5#	A24	Indicates system is in Soft off state. Same signal as SUS_S4#.
WAKE0#	B66	PCI Express wake up request signal.
WAKE1#	B67	General purpose wake up signal. May be used to implement a wake-up request from an external device.
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.

Table 21: Thermal Protection Interface Signal Descriptions

Signal	COM Express Pin Number	Description
THRM#	B35	Input from off-module temp sensor indicating an over temperature situation.
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.

Table 22: SM Bus Signal Descriptions

Signal	COM Express Pin Number	Description
SMB_CK	B13	System Management Bus bidirectional clock line
SMB_DAT	B14	System Management Bus bidirectional data line
SMB_ALERET#	B15	System Management Bus Alert - Active low input can be used to generate an SMI# (System Management Interrupt)

Table 23: General Purpose I/O Signal Descriptions

Signal	COM Express Pin Number	Description
GPI0	A54	General purpose input pin. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal
GPI1	A63	General purpose input pin. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal
GPI2	A67	General purpose input pin. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal
GPI3	A85	General purpose input pin. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.
GPO0	A93	General purpose output pin. Shared with SD_CLK. Output from COM Express, input to SD
GPO1	B54	General purpose output pin. Shared with SD_CMD. Output from COM Express, input to SD
GPO2	B57	General purpose output pin. Shared with SD_WP. Output from COM Express, input to SD
GPO3	B63	General purpose output pin. Shared with SD_CD. Output from COM Express, input to SD

Table 24: SDIO Signal Descriptions

Signal	COM Express Pin Number	Description
SDIO_CD#	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support
SDIO_CLK	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.
SDIO_CMD	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1.
SDIO_WP	B54	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support
SDIO_DAT0	A54	SDIO Data line. Operates in push-pull mode and maps to GPI0
SDIO_DAT1	A63	SDIO Data line. Operates in push-pull mode and maps to GPI1
SDIO_DAT2	A67	SDIO Data line. Operates in push-pull mode and maps to GPI2
SDIO_DAT3	A85	SDIO Data line. Operates in push-pull mode and maps to GPI3

Table 25: Module Type Definition Signal Descriptions

Signal	COM Express Pin Number	Description
TYPE10#	A97	Indicates to the baseboard that a Type 10 module is installed.

Table 26: Power and Ground Signal Descriptions

Signal	COM Express Pin Number	Description
VCC_12V	A104-A09 B104-B109	Primary power input: 4.75V to 20V. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_STBY	B84-B87	Standby power input: +5V nominal. If VCC5V_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Real time clock circuit-power input: +3 VDC nominal
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110 B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to baseboard GND plane.

Table 27: CAN Bus Signal Descriptions

Signal	COM Express Pin Number	Description
CAN0_TX	A101	Controller Area Network TX output for CAN Bus channel 0. This pin is shared with SER1_TX. (Not supported)
CAN0_RX	A102	Controller Area Network RX input for CAN Bus channel 0. This pin is shared with SER1_RX. (Not supported)

Appendix A – Mounting Options

A

VL-COMm-33 Mounting Configuration

Figure 11 shows the heat plate mounting configuration for the VL-COMm-33.

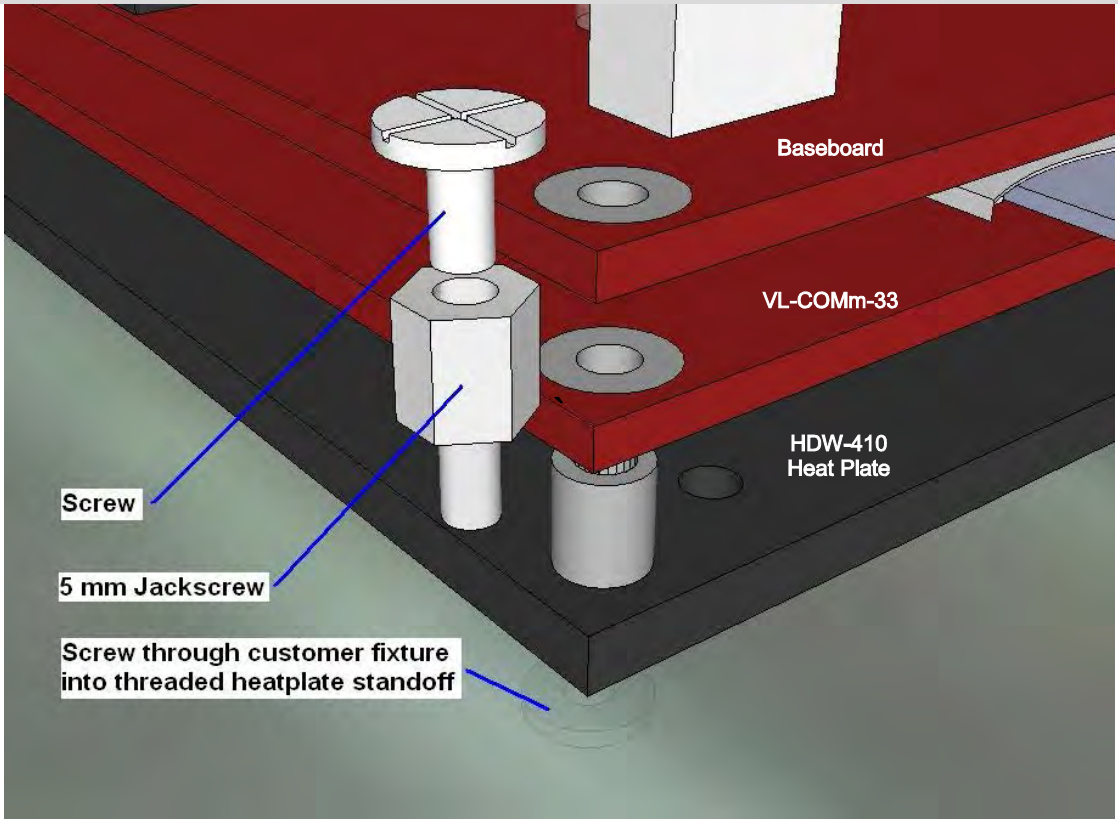


Figure 11. Bolt-through Heat Plate

Mounting Plate Configurations

Figure 12 and Figure 13 show options for installing the VL-COMm-33 with the VL-HDW-405 mounting plate.

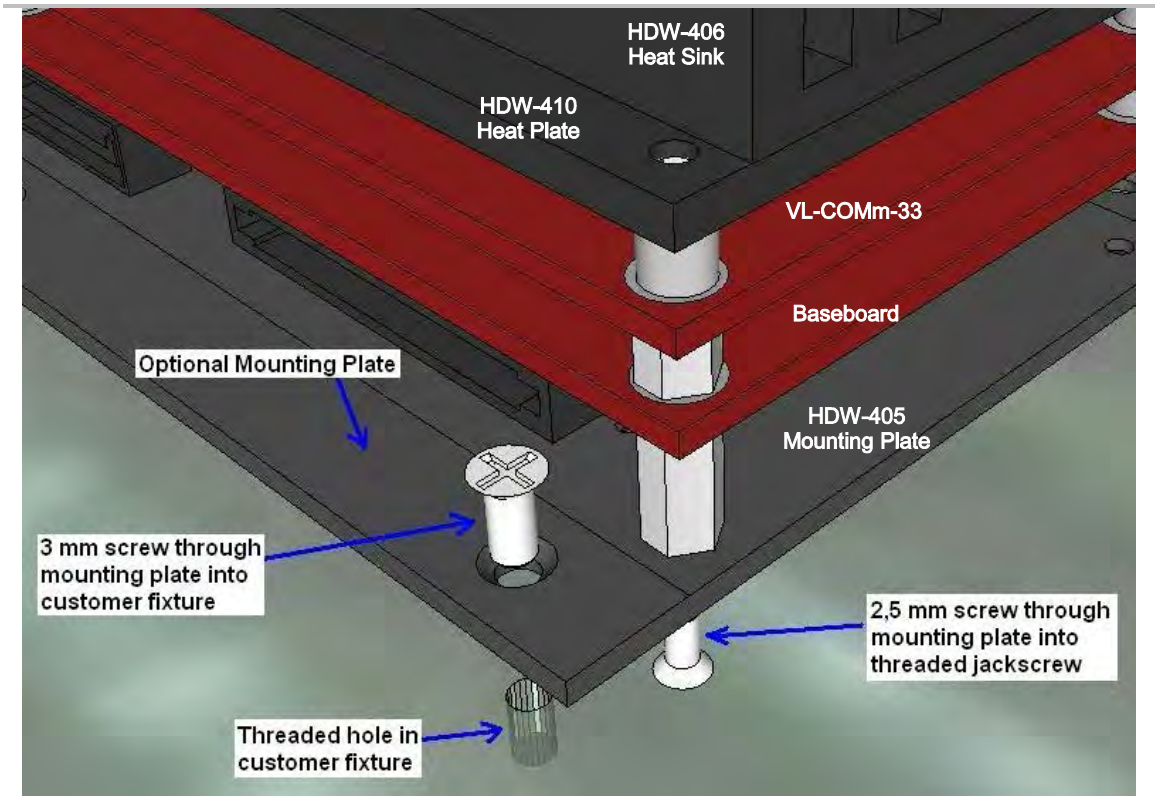


Figure 12. Mounting Plate Option 1

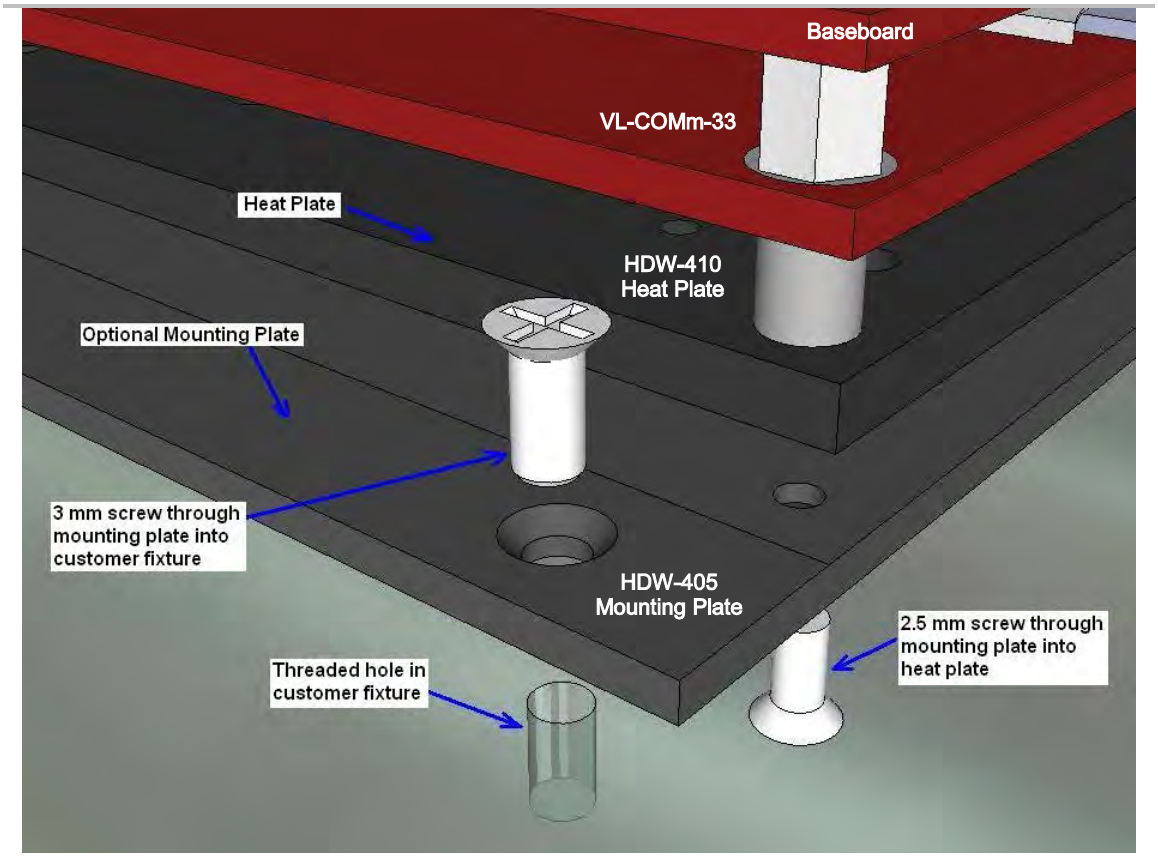


Figure 13. Mounting Plate Option 2

Attaching the Heat Plate to the VL-COMm-33

Figure 14 shows the items used to attach the heat plate to the COMm-33.

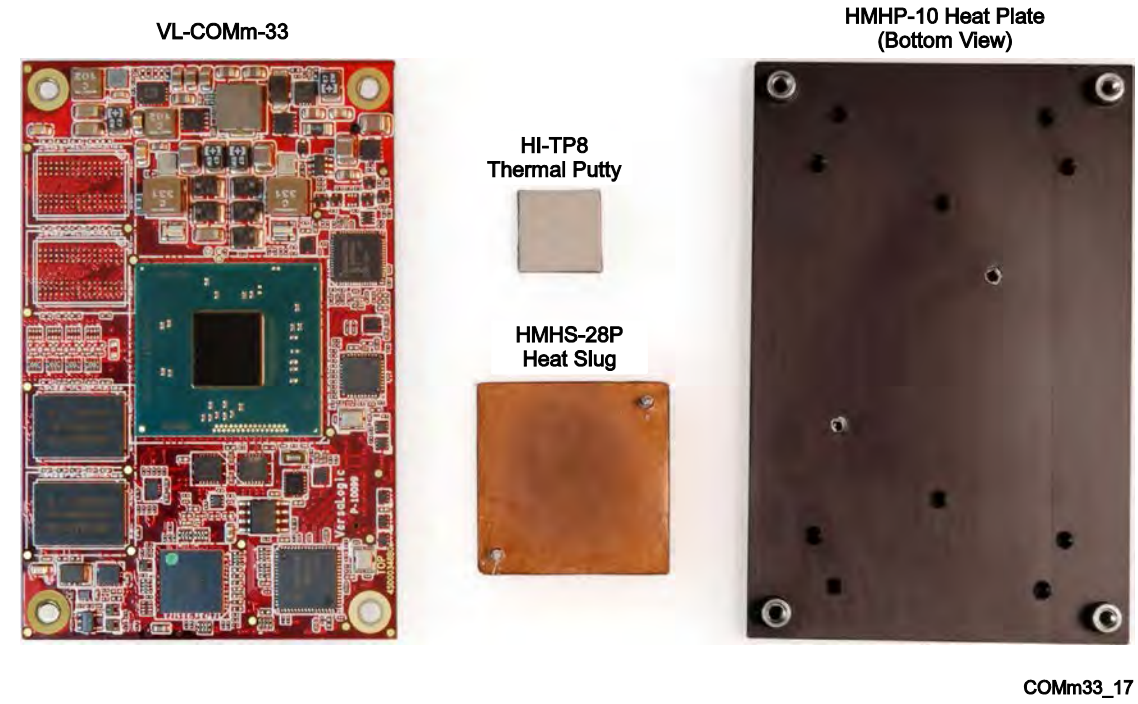


Figure 14. Items for Heat Plate Assembly

PLACING THE THERMAL PUTTY ON THE HEAT SLUG

Before beginning assembly, remove the plastic covering from the thermal putty. Place the thermal putty on the heat slug. The thermal putty should be centered on the heat slug and placed on the same side as the locating pins, as shown in Figure 15.

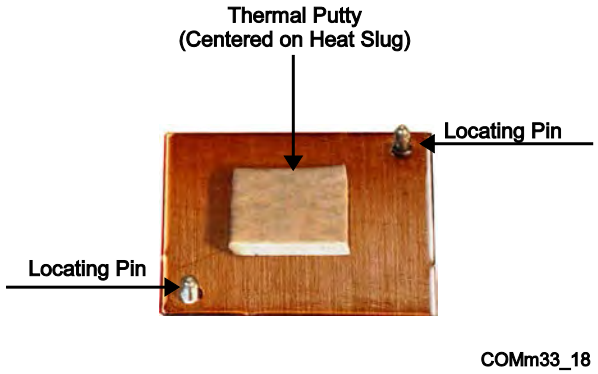


Figure 15. Placement of the Thermal Putty on the Heat Slug

ALIGNING THE HEAT SLUG WITH THE HEAT PLATE

Align the locating pins of the heat slug with the corresponding holes in the heat plate, as shown in Figure 16

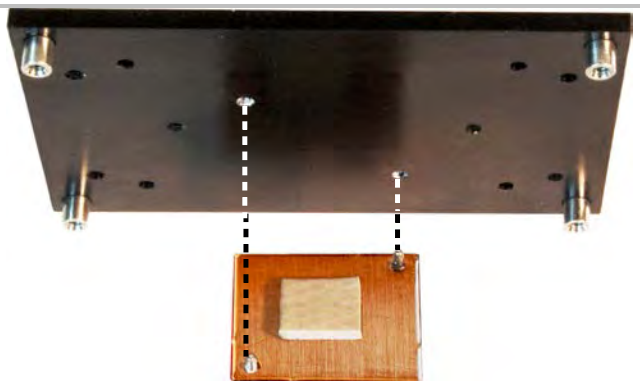


Figure 16. Aligning the Heat Slug's Locating Pins with the Heat Plate

Place the heat slug onto the heat plate, as shown in Figure 17. The locating pins will insert into the heat plate. The locating pins do not snap into the heat plate; the pins only rest in the holes. Do not squeeze the heat slug onto the heat plate; the stickiness of the putty should hold the heat slug snugly against the heat plate.

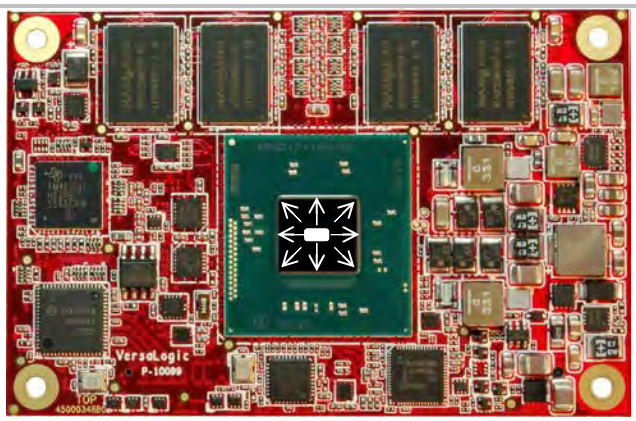
The locating pins help to keep the heat slug from shifting along either the x- or y-axis after the assembly is complete, ensuring reliable surface contact between the heat slug and the CPU die.

Figure 17. Fitting the Heat Slug to the Heat Plate

APPLYING THERMAL GREASE TO THE CPU DIE

Apply the HI-TAS5 Thermal Grease to the center of the CPU die. Apply the approximate volume of half a grain of rice.

Using a spreader stick, smooth the thermal grease to a uniform level covering the entire die surface as shown in Figure 18.



COMm33_21

Figure 18. Application Pattern for Thermal Grease on CPU Die

ALIGNING THE HEAT PLATE WITH THE COMM-33 BOARD

Before attaching the heat plate/thermal putty/slug assembly to the COMm-33 board, refer to Figure 19. The figure shows that both the slug on the heat plate and the CPU die on the COMm-33 board are not centered on their respective platforms; both have a noticeable offset (Dimension A being greater than Dimension B).

Before physically mating the two assemblies, be certain that the orientation of the heat plate matches that of the COMm-33 board. Proper alignment and orientation are necessary for optimum contact and adhesion between the heat plate and the CPU die.

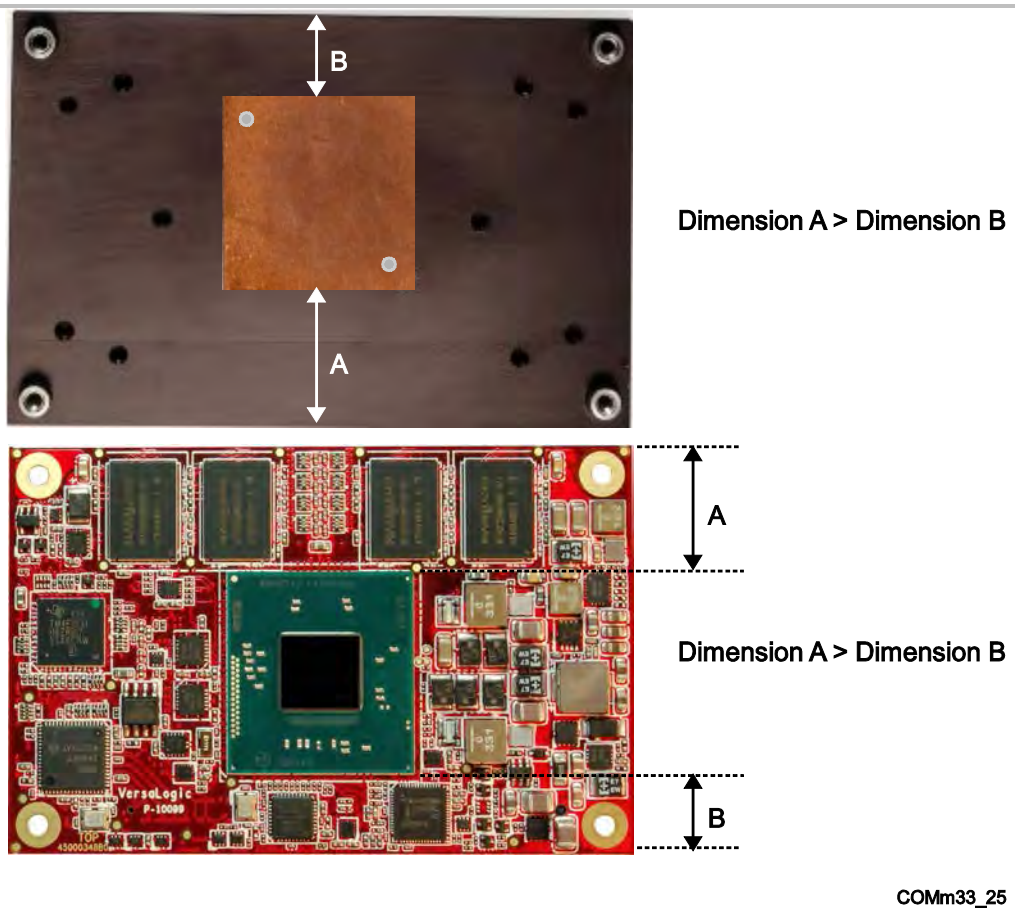


Figure 19. Offset of CPU Die and Heat Plate-Mounted Slug

After you have properly aligned the heat plate so that the heat slug is centered over the CPU die, carefully lower the heat plate into position, keeping the outside mounting holes aligned as shown in Figure 20.

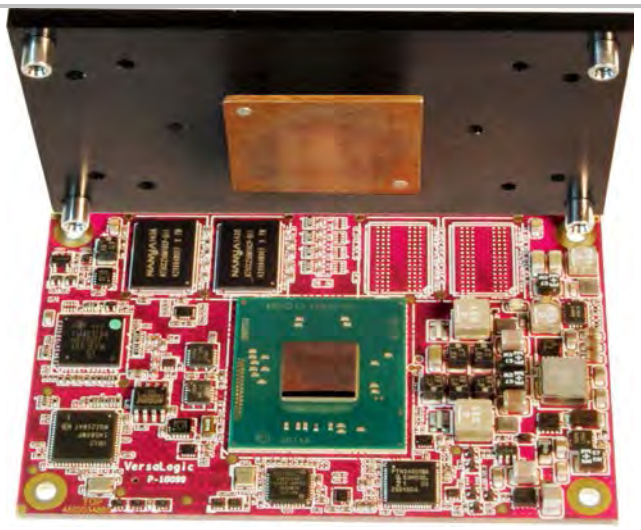


Figure 20. Positioning the Heat Plate and Slug Over the COMm-33

ATTACHING THE HEAT PLATE ASSEMBLY TO THE COMM-33

Keeping both sides aligned, invert the COMm-33 and the heat plate assembly. Install four HTSPM2505 standoffs, as shown in Figure 21. Use Loctite (HI-SG4) Thread Locker on all screws. Gently snug each screw, working around the board. Repeat until all screws are snug. Final torque should not exceed 4-inch lb.

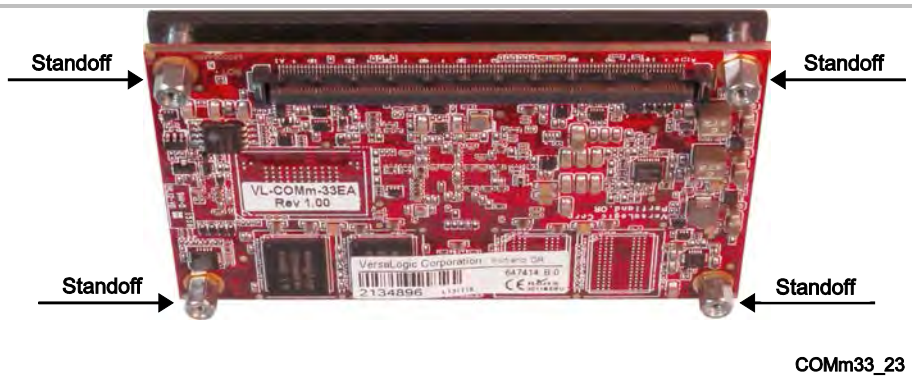


Figure 21. Location of Standoffs

Figure 22 provides a side view of the completed assembly.

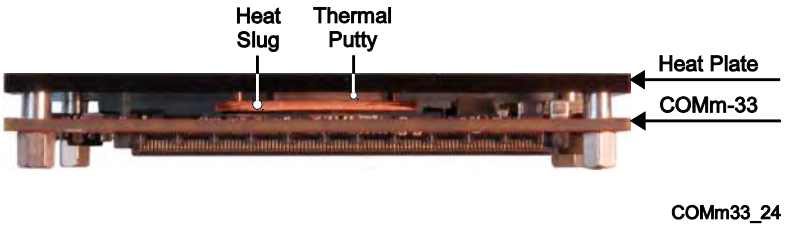


Figure 22. Side View of Completed Assembly