Low-Voltage Dual SPST Analog Switch

DESCRIPTION

The DG9262, DG9263 is a single-pole/single-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 35 ns, t_{OFF}: 20 ns), low on-resistance ($R_{DS(on)}$: 40 Ω) and small physical size, the DG9262, DG9263 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9262, DG9263 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7 is 2000 V. An epitaxial layer prevents latchup. Break-before make is guaranteed for DG9262, DG9263.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

FEATURES

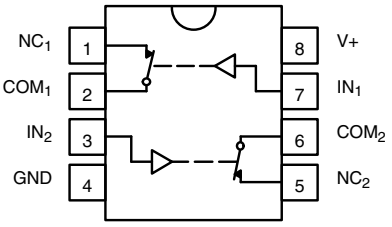
- **Halogen-free According to IEC 61249-2-21 Definition**
- Low Voltage Operation (- 2.7 V to 5 V)
- Low On-Resistance - $R_{DS(on)}$: 40 Ω
- Fast Switching - t_{ON}: 35 ns, t_{OFF}: 20 ns
- Low Leakage - $I_{COM(on)}$: 200-pA max.
- Low Charge Injection - Q_{INJ}: 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in MSOP-8 and SOIC-8
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free Available
RoHS* COMPLIANT
HALOGEN FREE

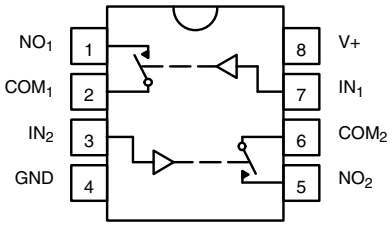
APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



Top View

TRUTH TABLE - DG9262	
Logic	**Switch**
0	On
1	Off

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9263	
Logic	**Switch**
0	Off
1	On

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	SOIC-8	DG9262DY-E3 DG9262DY-T1 DG9262DY-T1-E3
		DG9263DY-E3 DG9263DY-T1 DG9263DY-T1-E3
	MSOP-8	DG9262DQ-T1-E3
		DG9263DQ-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 13	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 20	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 40	
ESD (Method 3015.7)		> 2000	V
Storage Temperature (D Suffix)		- 65 to 125	°C
Power Dissipation (Packages)[b]	8-Pin Narrow Body SOIC[c]	400	mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75 °C.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	Temp.[a]	D Suffix - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V, V+ = 2.7 V I_{COM} = 5 mA	Room Full		50	80 140	Ω
$R_{DS(on)}$ Match[d]	$\Delta R_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room		0.4	2	
$R_{DS(on)}$ Flatness[d]	$R_{DS(on)}$ Flatness	V_{NO} or V_{NC} = 1 and 2 V	Room		4	8	
NO or NC Off Leakage Current[g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V/2 V, V_{COM} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	pA
COM Off Leakage Current[g]	$I_{COM(off)}$	V_{COM} = 1 V/2 V, V_{NO} or V_{NC} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	
Channel-On Leakage Current[g]	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V/2 V	Room Full	- 200 - 10 000	10	200 10 000	
Digital Control							
Input Current	I_{INL} or I_{INH}		Full		1		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V	Room Full		50	120 200	ns
Turn-Off Time	t_{OFF}		Room Full		20	50 120	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		1	5	pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X_{TALK}		Room		- 90		
NC and NO Capacitance	$C_{(off)}$	f = 1 MHz	Room		7		pF
Channel-On Capacitance	$C_{COM(on)}$		Room		20		
COM-Off Capacitance	$C_{COM(off)}$		Room		13		
Power Supply							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 3.3 V, V_{IN} = 0 V or 3.3 V				1	µA

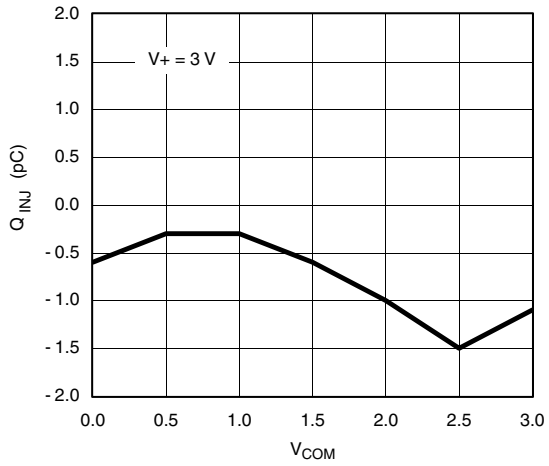
Notes:
a. Room = 25 °C, full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.
g. Gurauranteed by 5 V leakage testing, not production tested.

SPECIFICATIONS (V+ = 5 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	**Temp.[a]**	**D Suffix - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V, V+ = 4.5 V I_{COM} = 5 mA	Room Full		30	60 75	Ω
$R_{DS(on)}$ Match[d]	$\Delta R_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V	Room		0.4	2	
$R_{DS(on)}$ Flatness[f]	$R_{DS(on)}$ Flatness	V_{NO} or V_{NC} = 1, 2 and 3 V	Room		2	6	
NO or NC Off Leakage Current	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V/4 V, V_{COM} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	pA
COM Off Leakage Current	$I_{COM(off)}$	V_{COM} = 1 V/4 V, V_{NO} or V_{NC} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	
Channel-On Leakage Current	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V/4 V	Room Full	- 200 - 10 000		200 10 000	
Digital Control							
Input Current	I_{INL} or I_{INH}		Full		1		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3 V	Room Full		35	75 150	ns
Turn-Off Time	t_{OFF}		Room Full		20	50 100	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		2	5	pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X_{TALK}		Room		- 90		
NC and NO Capacitance	$C_{(off)}$	f = 1 MHz	Room		7		pF
Channel-On Capacitance	$C_{D(on)}$		Room		20		
COM-Off Capacitance	$C_{COM(off)}$		Room		13		
Power Supply							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 V or 5.5 V				1	µA

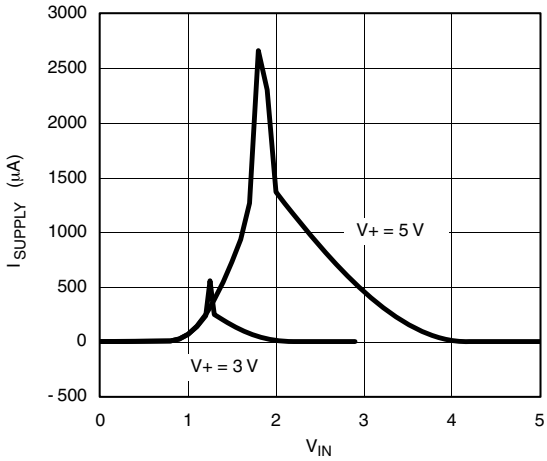
Notes:
a. Room = 25 °C, full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

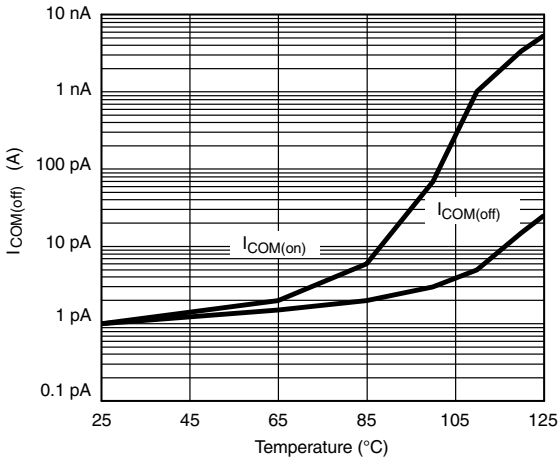
TYPICAL CHARACTERISTICS (25°C, unless otherwise noted)



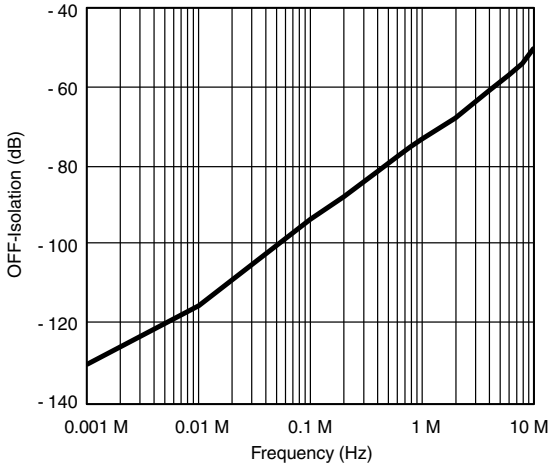
Charge Injection



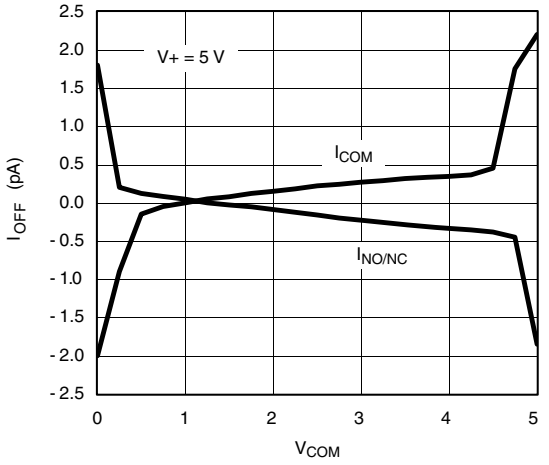
Supply Current vs. V_{IN}



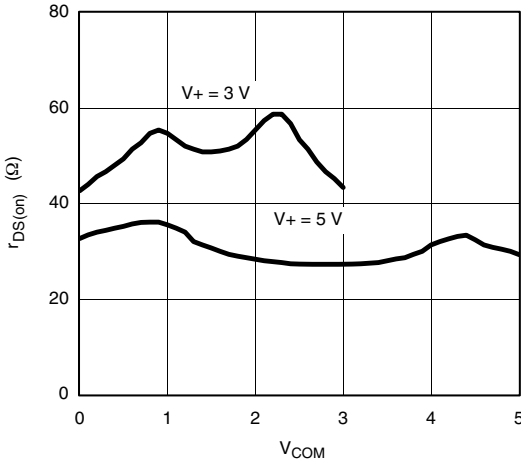
Leakage Current vs. Temperature



Off-Isolation vs. Frequency

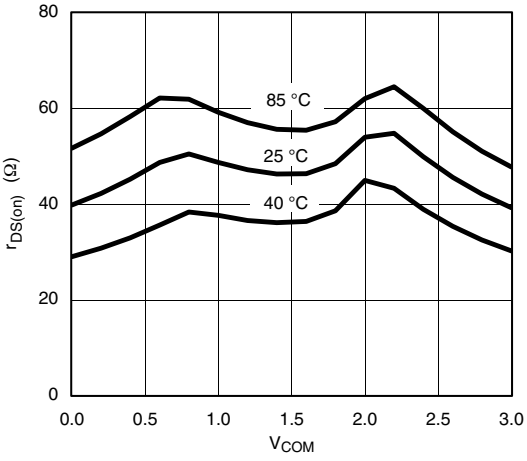


Off-Leakage vs. Voltage at 25 °C

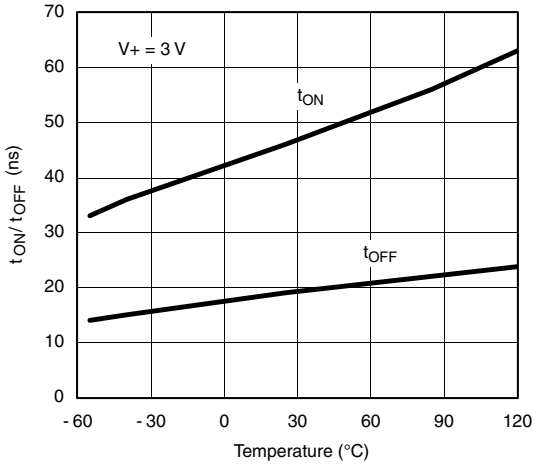


R_{DS} vs. V_{COM}

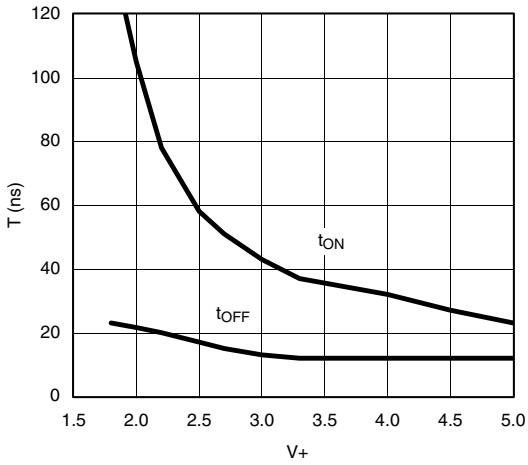
TYPICAL CHARACTERISTICS (25°C, unless otherwise noted)



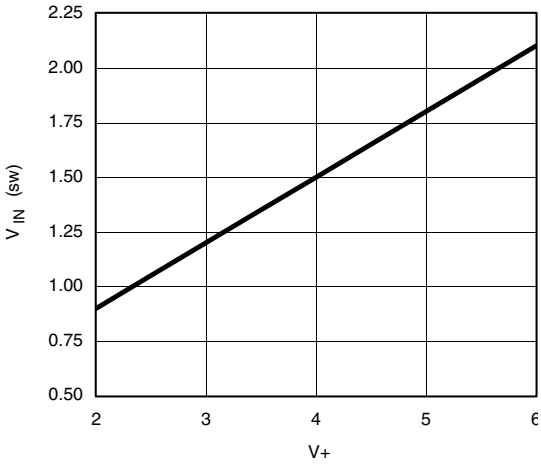
R_{DS} vs. V_{COM}



Switching Time vs. Temperature

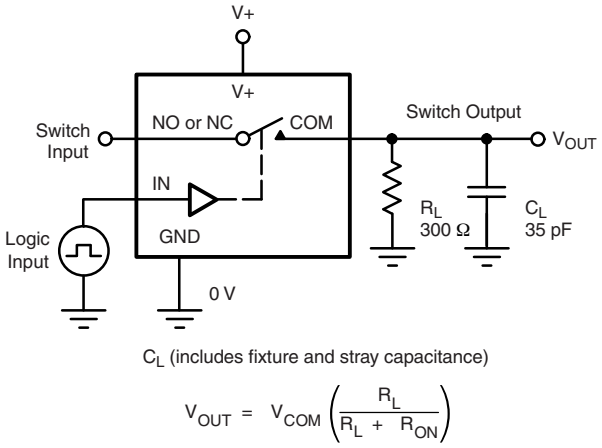


t_{ON}/t_{OFF} vs. Power Supply Voltage



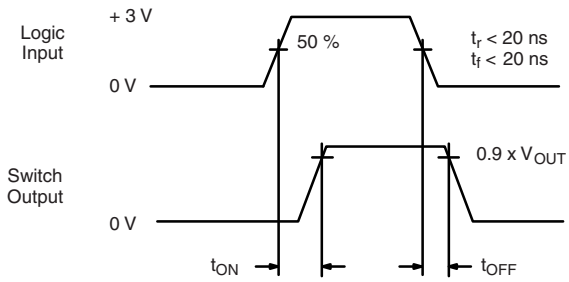
Input Switching Point vs. Power Supply Voltage

TEST CIRCUITS



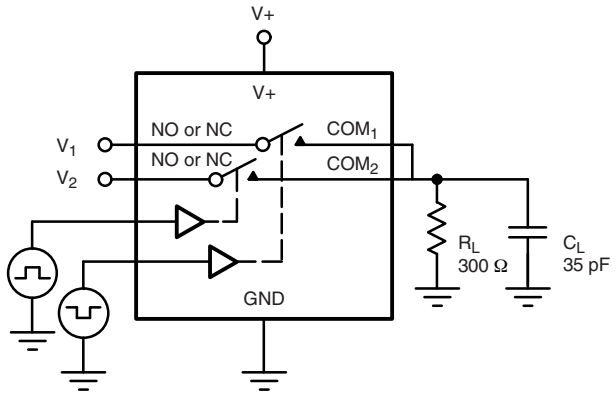
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

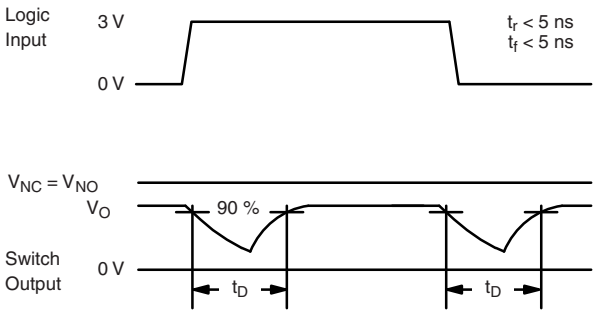
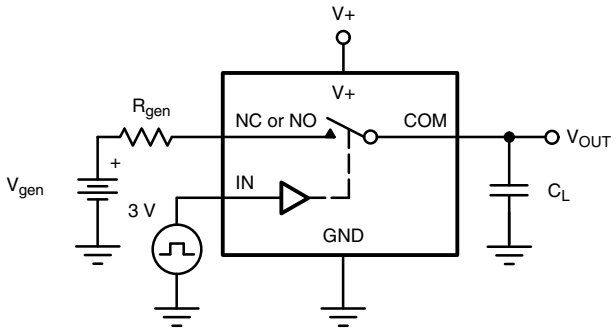
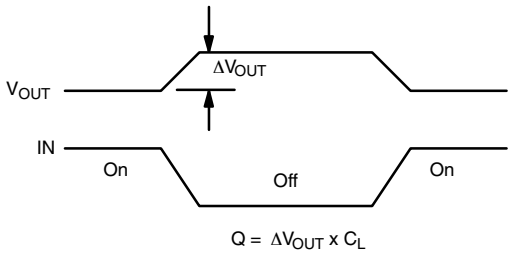


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

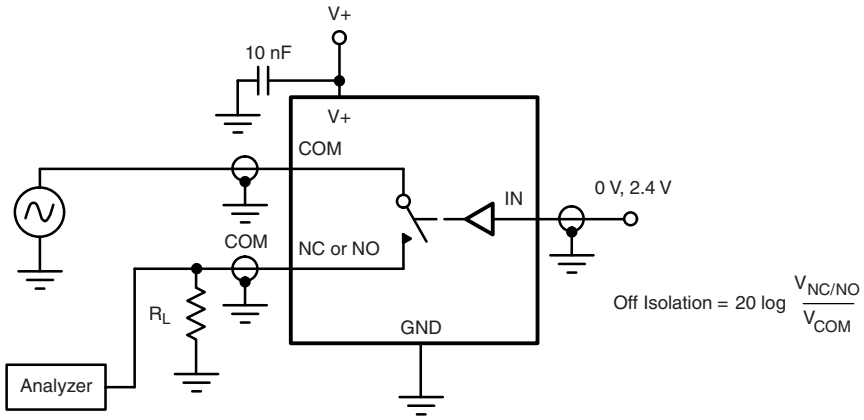


Figure 4. Off-Isolation

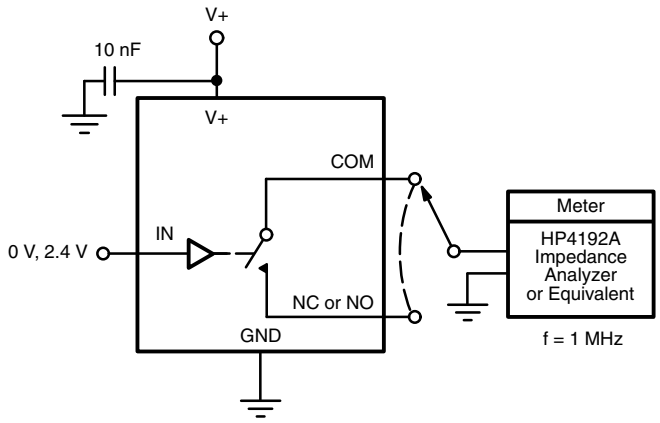
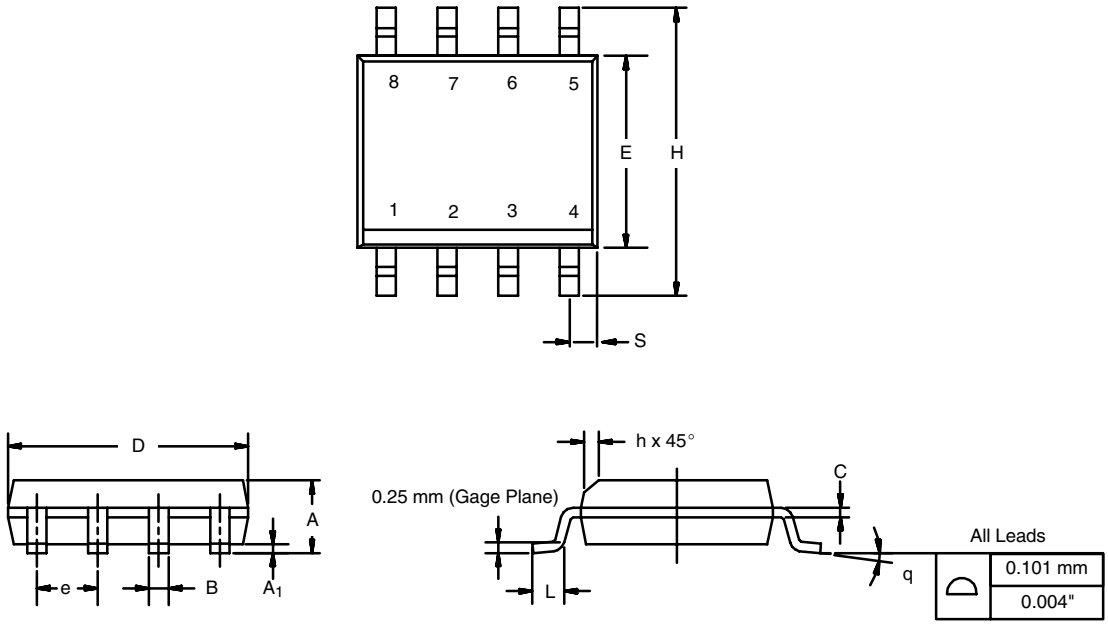


Figure 5. Channel Off/On Capacitance

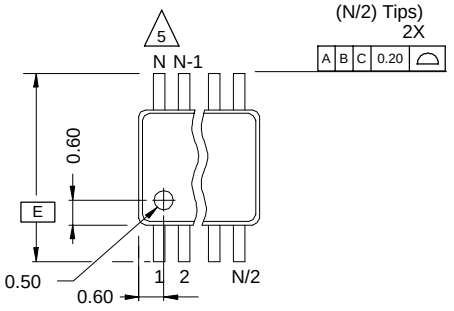
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



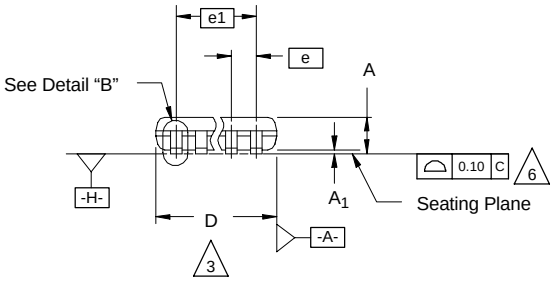
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

MSOP: 8-LEADS

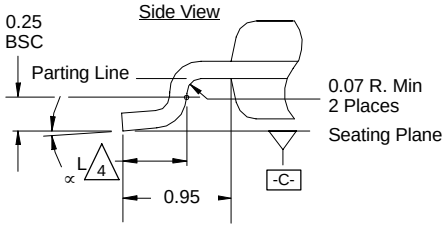
JEDEC Part Number: MO-187, (Variation AA and BA)



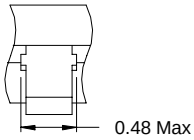
Top View



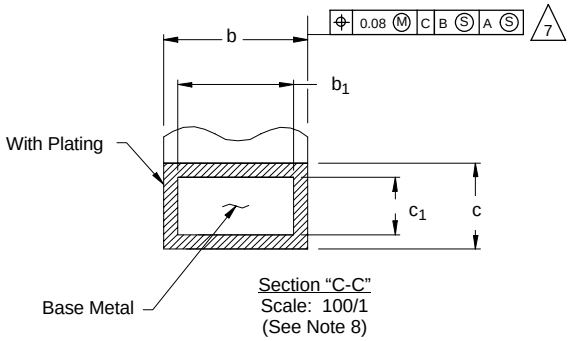
Side View



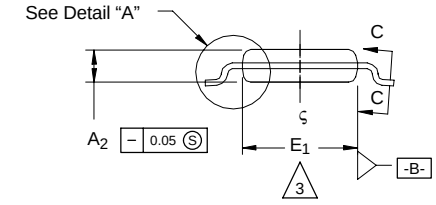
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.25	-	0.38	8
b_1	0.25	0.30	0.33	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.65 BSC			
e_1	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

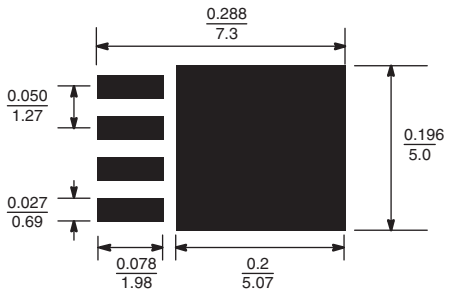


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

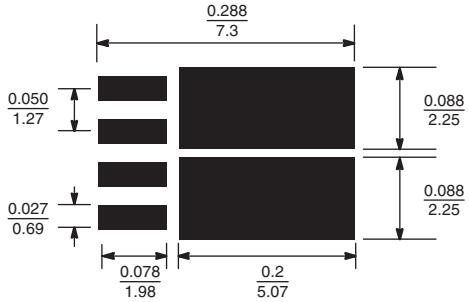


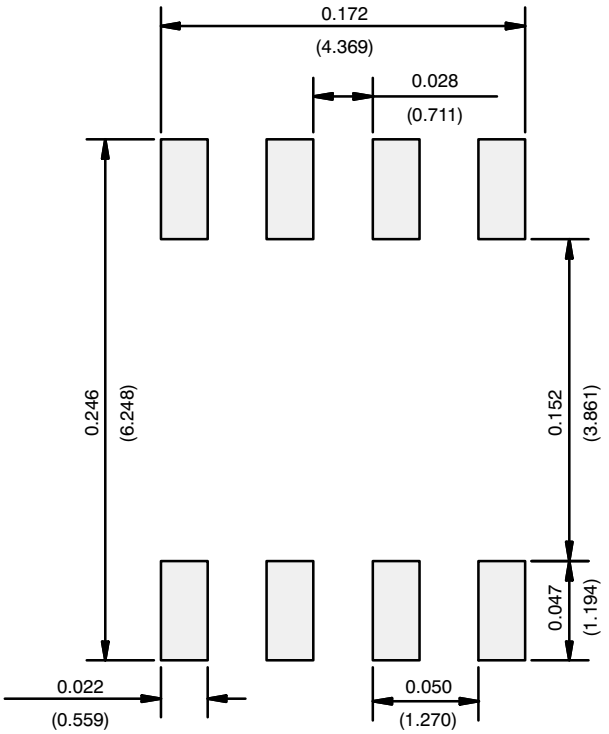
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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