Phase Detector/Frequency Synthesizer

ADF4002-EP

FEATURES

400 MHz bandwidth
2.7 V to 3.3 V power supply
Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
Programmable charge pump currents
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode
104 MHz phase frequency detector
Supports defense and aerospace applications (AQEC standard)
Military temperature range: −55°C to +125°C
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Clock conditioning
Clock generation
IF LO generation

GENERAL DESCRIPTION

The ADF4002-EP frequency synthesizer is used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, and a programmable N divider. The 14-bit reference counter (R counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). In addition, by programming R and N to 1, the part can be used as a stand-alone PFD and charge pump.

Additional application and technical information can be found in the ADF4002 data sheet.

FUNCTIONAL BLOCK DIAGRAM

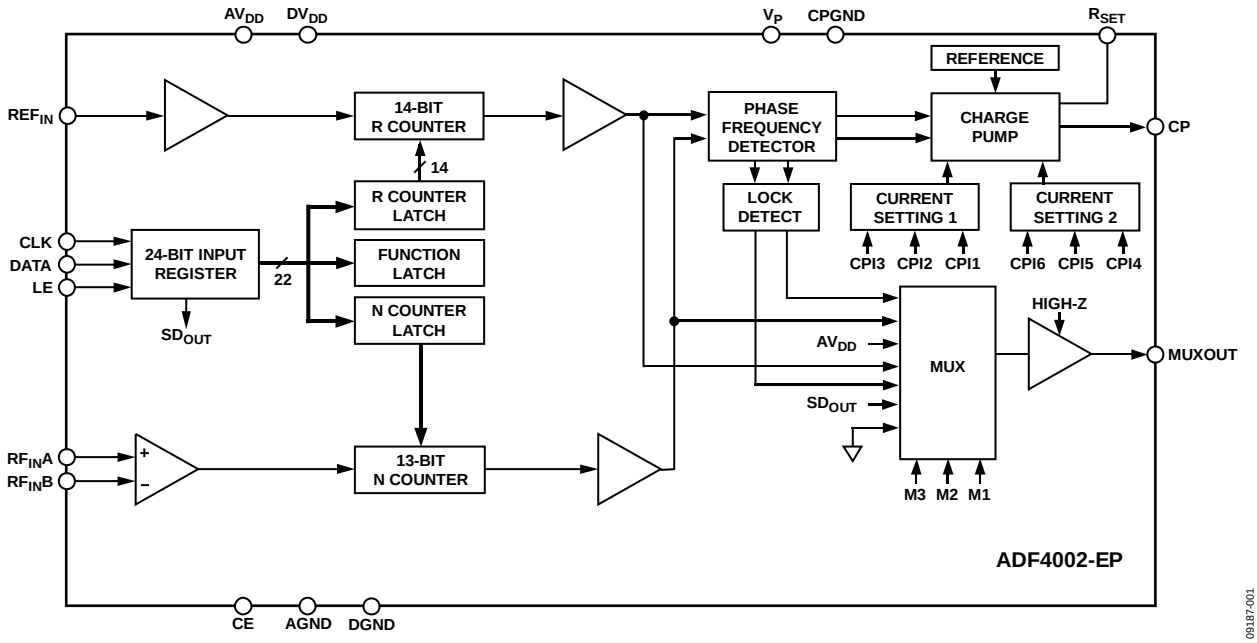

Figure 1.

Rev. 0

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REVISION HISTORY

11/10—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, AV_{DD} ≤ V_P ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted. Operating temperature range is −55°C to +125°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
RF Input Sensitivity	−10		0	dBm	
RF Input Frequency (RF_{IN})	5		400	MHz	For RF_{IN} < 5 MHz, ensure slew rate (SR) > 4 V/µs
REF_{IN} CHARACTERISTICS					
REF_{IN} Input Frequency	20		300	MHz	For REF_{IN} < 20 MHz, ensure SR > 50 V/µs
REF_{IN} Input Sensitivity[1]	0.8		AV_{DD}	V p-p	Biased at AV_{DD}/2 (ac coupling ensures AV_{DD}/2 bias)
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE FREQUENCY DETECTOR (PFD)					
Phase Detector Frequency[2]			104	MHz	ABP[2:1] = 00 (2.9 ns antibacklash pulse width)
CHARGE PUMP					Programmable
I_{CP} Sink/Source					
High Value		5		mA	R_{SET} = 5.1 kΩ
Low Value		625		µA	
Absolute Accuracy		2.5		%	R_{SET} = 5.1 kΩ
R_{SET} Range	3.0		11	kΩ	
I_{CP} Three-State Leakage		1		nA	T_A = 25°C
I_{CP} vs. V_{CP}		1.5		%	0.5 V ≤ V_{CP} ≤ (V_P − 0.5 V)
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ (V_P − 0.5 V)
I_{CP} vs. Temperature		2		%	V_{CP} = V_P/2
LOGIC INPUTS					
Input High Voltage, V_{IH}	1.4			V	
Input Low Voltage, V_{IL}			0.6	V	
Input Current, I_{INH}, I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	1.4			V	Open-drain output, 1 kΩ pull-up resistor to 1.8 V
	DV_{DD} − 0.4			V	CMOS output
Output High Current, I_{OH}			100	µA	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}	AV_{DD}			V	
V_P	AV_{DD}		5.5	V	AV_{DD} ≤ V_P ≤ 5.5 V
I_{DD}[3] (AI_{DD} + DI_{DD})		5.0	6.0	mA	
I_P			0.4	mA	T_A = 25°C
Power-Down Mode		1		µA	AI_{DD} + DI_{DD}
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor (PN_{SYNTH})[4, 5]		−222		dBc/Hz	PLL loop bandwidth = 500 kHz
Normalized 1/f Noise (PN_{1_f})[4, 6]		−119		dBc/Hz	Measured at 10 kHz offset; normalized to 1 GHz

[1] AV_{DD} = DV_{DD} = 3 V.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; RF_{IN} = 350 MHz. The current for any other setup (25°C, 3.0 V) in mA is given by 2.35 + 0.0046 (REF_{IN}) + 0.0062 (RF); RF frequency and REF_{IN} frequency in MHz.
[4] All phase noise measurements were performed with a Rohde & Schwarz FSUP26 phase noise test system using the EVAL-ADF4002EBZ1 evaluation board and the ultralow noise, 100 MHz OCXO from Wenzel (Part No. 501-16843) as the PLL reference.
[5] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value) and 10logf_{PFD}. PN_{SYNTH} = PN_{TOT} − 10logf_{PFD} − 20logN.
[6] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by PN = P_{1_f} + 10log(10 kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and the flicker noise are modeled in ADIsimPLL.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = 3 V ± 10%, AV_{DD} ≤ V_P ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted. Operating temperature range is −55°C to +125°C.

Table 2.

Parameter	Limit[1]	Unit	Description
t_1	10	ns min	DATA to CLK setup time
t_2	10	ns min	DATA to CLK hold time
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time
t_6	20	ns min	LE pulse width

[1] Guaranteed by design, but not production tested.

Timing Diagram

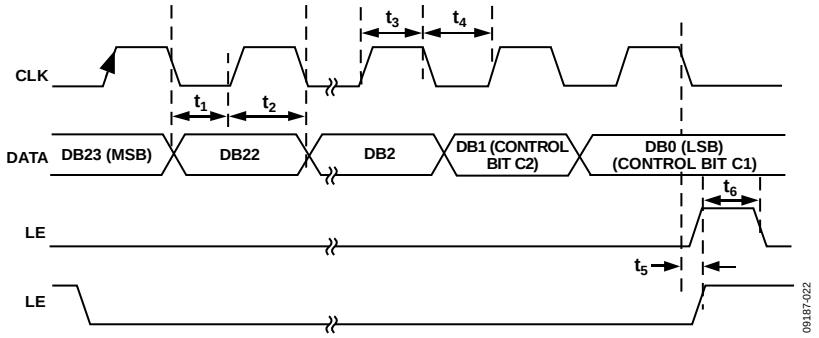


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND[1]	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND[1]	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND[1]	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−55°C to +125°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = CPGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

THERMAL CHARACTERISTICS

Table 4. Thermal Impedance

Package Type	θ_{JA}	Unit
TSSOP (RU-16)	150.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

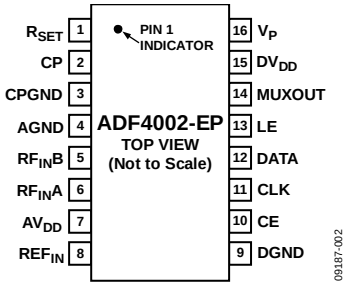


Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{25.5}{R_{SET}}$$ where R_{SET} = 5.1 kΩ and $I_{CP\,MAX}$ = 5 mA.
2	CP	Charge Pump Output. When enabled, this output provides ±I_{CP} to the external loop filter that, in turn, drives the external VCO.
3	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	AGND	Analog Ground. This is the ground return path of the RF input.
5	$RF_{IN}B$	Complementary Input to the RF Input. This pin must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	$RF_{IN}A$	Input to the RF Input. This small-signal input is ac-coupled to the external VCO.
7	AV_{DD}	Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to the AV_{DD} pin. AV_{DD} must be the same value as DV_{DD}.
8	REF_{IN}	Reference Input. This CMOS input has a nominal threshold of AV_{DD}/2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	DGND	Digital Ground.
10	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking this pin high powers up the device, depending on the status of the Power-Down Bit PD1.
11	CLK	Serial Clock Input. The serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first; the two LSBs are the control bits. This input is a high impedance CMOS input.
13	LE	Load Enable. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits. This input is a high impedance CMOS input.
14	MUXOUT	Multiplexer Output. This output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	DV_{DD}	Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to the DV_{DD} pin. DV_{DD} must be the same value as AV_{DD}.
16	V_P	Charge Pump Power Supply. This should be greater than or equal to AV_{DD}. In systems where AV_{DD} is 3 V, V_P can be set to 5.5 V and used to drive a VCO with a tuning voltage of up to 5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

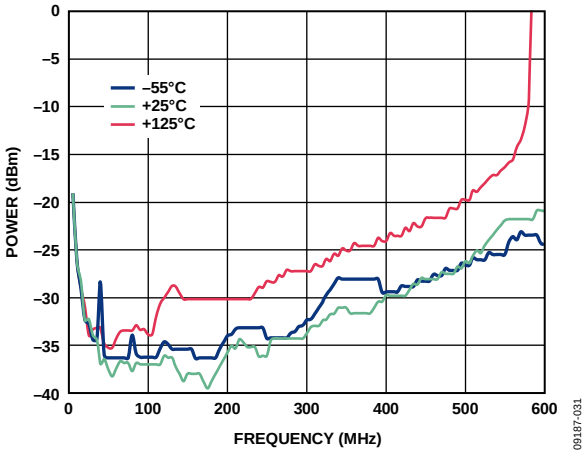


Figure 4. RF Input Sensitivity

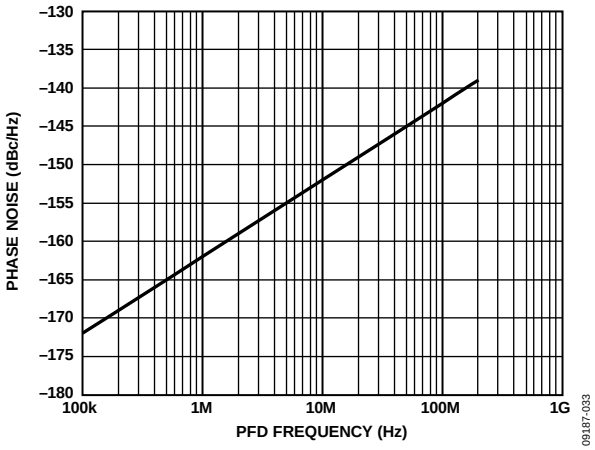


Figure 7. Phase Noise (Referred to CP Output) vs. PFD Frequency

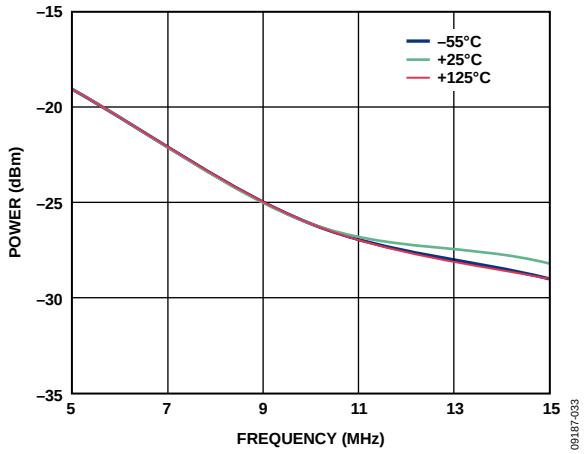


Figure 5. RF Input Sensitivity, Low Frequency

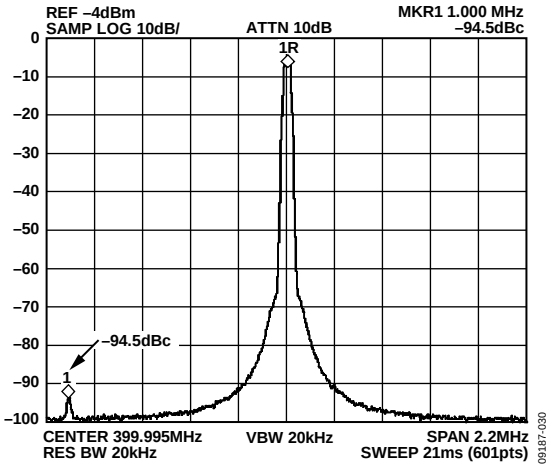


Figure 8. Reference Spurs (400 MHz, 1 MHz, 7 kHz)

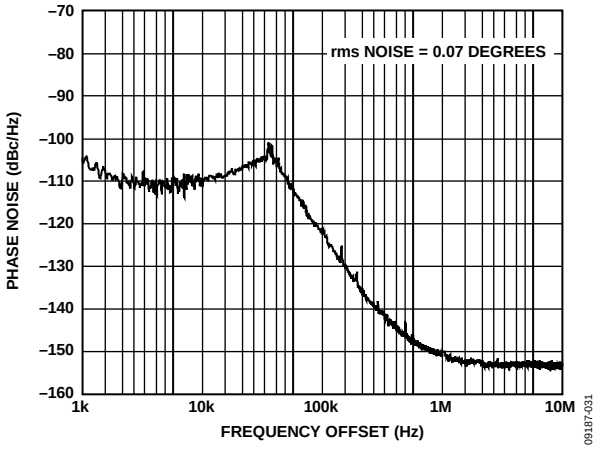
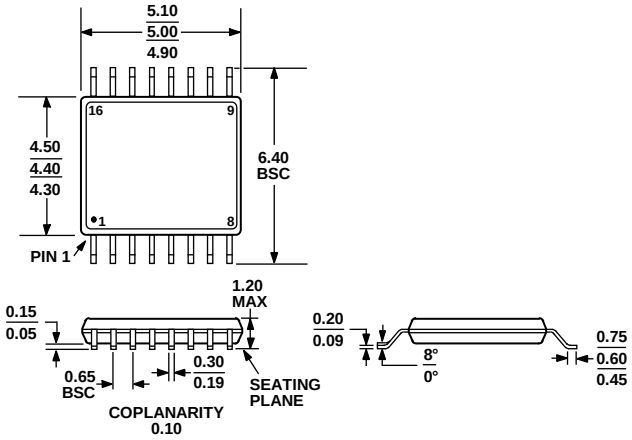


Figure 6. Integrated Phase Noise (400 MHz, 1 MHz, 50 kHz)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 9. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4002SRU-EP	−55°C to +125°C	16-Lead TSSOP	RU-16
ADF4002SRU-EP-RL7	−55°C to +125°C	16-Lead TSSOP	RU-16

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