ANALOG DEVICES

AD8233CB-EBZ User Guide
UG-1016

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Evaluating the AD8233 50 µA, 2 mm × 1.7 mm WLCSP, Low Noise, Heart Rate Monitor for Wearable Products

FEATURES

Ready to use HRM front end
Operates in two-electrode or three-electrode configurations
Directly interfaces to data acquisition and analog-to-digital converters (ADCs)
Easy mode selection with switches
Allows various circuit configurations
3.5 mm electrode jack

EVALUATION KIT CONTENTS

AD8233CB-EBZ evaluation board

EQUIPMENT NEEDED

Power supply
Electrocardiogram (ECG) signal generator
Sensor cable (optional)

ONLINE RESOURCES

AD8233 data sheet
AD8233CB-EBZ user guide
AN-617 application note

GENERAL DESCRIPTION

The AD8233CB-EBZ evaluation board contains an AD8233 heart rate monitor (HRM) front end conveniently mounted with the necessary components for initial evaluation in fitness applications. Inputs, outputs, supplies, and leads off detection terminals are routed to test pins to simplify connectivity. Switches and jumpers are available for setting the input bias voltage, shutdown (SDN), right leg drive shutdown (RLD SDN), fast restore (FR), and ac/dc leads off detection mode.

The AD8233CB-EBZ evaluation board is a 4-layer board with components mounted on the primary side only. Rubber feet are available on the secondary side for mechanical stability. The layout diagrams are provided as a visual aid and reference design. The printed circuit board (PCB) is designed following standard practices to ensure signal integrity and reduce manufacturing costs. For best WLCSP layout practices, refer to AN-617.

Full details about the AD8233 are available in the AD8233 data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using this evaluation board.

PHOTOGRAPH OF THE AD8233CB-EBZ EVALUATION BOARD

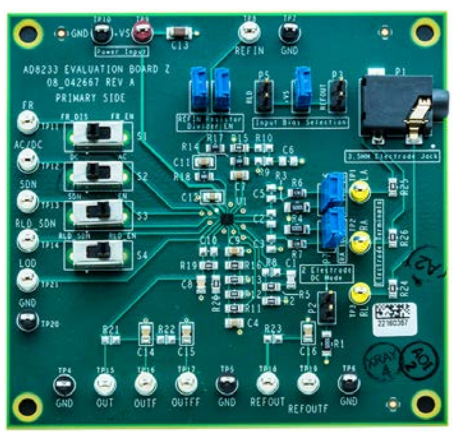

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Figure 1.

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REVISION HISTORY

8/2016—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

A simplified schematic is shown in Figure 2 of the AD8233CB-EBZ evaluation board default configuration. See the Evaluation Board Component Selection section for the full schematic. The expected output signal is measured at the OUT terminal, shown in Figure 3.

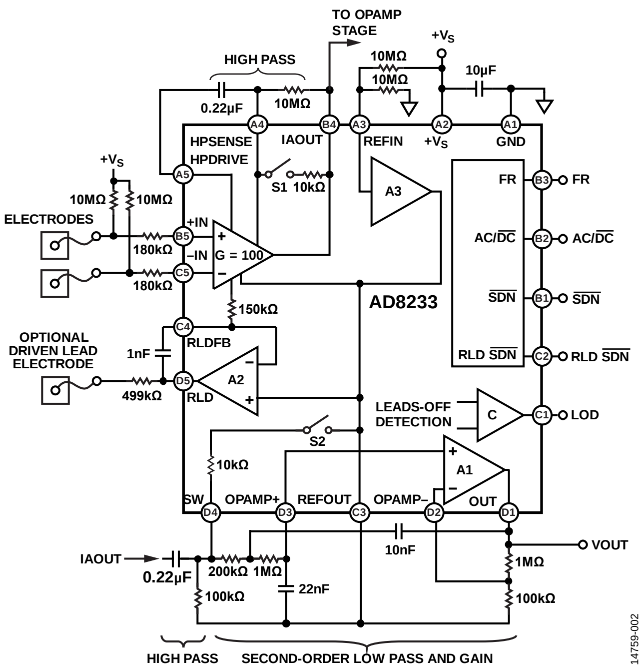

Figure 2. AD8233CB-EBZ Default Configuration

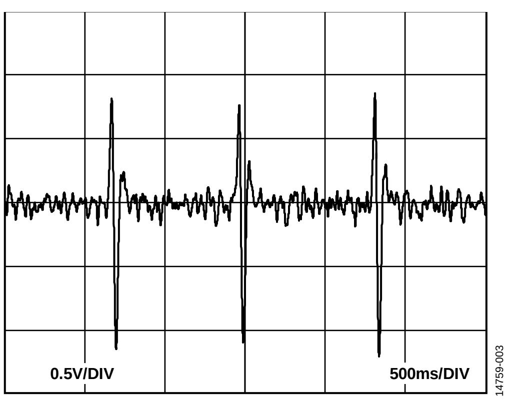

Figure 3. AD8233CB-EBZ Expected Output Signal Measured at the OUT Terminal

QUICK START GUIDE

The AD8233CB-EBZ evaluation board ships with a default configuration of a three-electrode system that connects to the hands of a subject. For a three-electrode configuration, verify the switches and jumpers are set to the default values shown in Table 1. Various other configurations are shown in Table 2.

Table 1. Default Switch and Jumper Settings

Label	Position	Setting
S1	FR_DIS	Fast restore disabled
S2	DC	DC leads off detection
S3	EN	Operation enabled
S4	RLD_EN	RLD enabled
Input Bias Selection	P4, P6, P7	Three-electrode dc
REFIN Resistor Divider EN	P8, P9	REFIN is set to $+V_S/2$

Setup Procedure

Take the following steps to set up the AD8233CB-EBZ evaluation board:

1. Connect a power supply common to the GND terminal on the evaluation board. Connect a +3 V supply voltage at the +VS terminal.
2. Connect the left arm (LA) terminal and the right arm (RA) terminal to a signal source such as an ECG signal generator.
3. Connect the right leg (RL) terminal to a signal source such as an ECG signal generator. The RLD is available via the RL terminal.
4. Alternatively, connect a sensor cable (not included) to the 3.5 mm electrode jack and connect the electrodes to a signal source such as an ECG signal generator.
5. The output signal is available on the OUT terminal. The expected output signal is shown in Figure 3.

Precaution When Using the AD8233CB-EBZ

For safety reasons, Analog Devices recommends evaluating the AD8233 with an ECG signal source instead of a live subject. Although the LA, RA, and RL electrode terminals are equipped with current-limiting resistors (R6 and R7), these resistors are not a comprehensive patient protection system. The resistors may not protect against supply line transients or leakage currents coming through power and acquisition systems. The user is fully responsible for understanding and applying all the safety guidelines and regulations that apply to medical equipment.

SIGNAL PATH—INSTRUMENTATION AMPLIFIER AND FILTERS

The AD8233CB-EBZ evaluation board ships with a default configuration for applications that involve three-electrodes connected to the hands. The LA, RA, and RL terminals serve as the signal inputs and the right leg drive electrode connections, respectively.

The instrumentation amplifier has a fixed gain of 100, and the operational amplifier is set for a gain of 11. The overall gain is 1100, which limits the maximum differential input signal to approximately 2.7 mV p-p. Exceeding this amplitude does not damage the AD8233; however, the signal at the output appears distorted. Due to the high Q of the filter, additional peaking sets the maximum observed gain more than 1100 at approximately 15 Hz. The total gain can be changed by adjusting the R19 and R20 resistors, but doing so has a direct impact on the Q of the low-pass filter. The instrumentation amplifier has a fixed gain of 100.

A single-supply configuration can implement the entire signal chain. For this purpose, the reference buffer is set to a ratiometric level at midsupply using two 10 MΩ resistors (R17 and R18) and the REFIN Resistor Divider EN jumpers (P8 and P9). The integrated reference buffer output provides a midsupply dc level for the system. The signal at the output rides on top of this midsupply level. This voltage is available at the REFOUT pin (TP18) to serve as a reference level for the subsequent signal acquisition stages. For different reference voltages, an external voltage can be applied to the REFIN pin. In this case, the REFIN Resistor Divider EN jumpers must be removed (P8 and P9).

The circuit implements a two-pole, high-pass filter for eliminating motion artifacts and the electrode half-cell potential. Additionally, the integrated operational amplifier creates a two-pole, low-pass filter to remove line noise and other interference signals. The frequency cutoff of all filters can be adjusted by changing component values.

It is possible the gain and filtering must need adjusting depending on the location of the electrodes and the application. Narrow bandwidths offer the highest rejection to motion artifacts and other external interferences; however, these bandwidths can introduce distortion into the ECG signal as shown in Figure 3. For more information, refer to the AD8233 data sheet.

The AD8233CB-EBZ evaluation board components selection is shown in the Evaluation Board Component Selection section and the Evaluation Board Schematic and Artwork section.

RIGHT LEG DRIVE (RLD) AMPLIFIER

The integrated RLD amplifier senses the common-mode voltage present at the signal inputs and can drive an opposing signal into the patient. This driven electrode functionality maintains a constant voltage between the patient and the AD8233, greatly improving the common-mode rejection ratio (CMRR).

The board configures the RLD amplifier as an integrator, formed by an internal 150 kΩ resistor and an external 1 nF capacitor (C1). This configuration results in a loop gain of approximately 20 at line frequencies with a crossover frequency of approximately 1 kHz.

In the ac mode two-electrode configuration, the RLD pin can drive the bias current resistors on the inputs. To create this connection, place a jumper at P5. In the dc mode two-electrode configuration, the RLD amplifier can be shut down to save power by positioning the S4 switch to RLD_SDN. In this mode, remove C1 and leave the RLD and RLDFB pins floating.

FILTER CONFIGURATIONS

The resistor and capacitor values for the filters on the AD8233CB-EBZ evaluation board provide effective noise rejection in applications that involve pulse detection while the subject is in motion. The filter parameters can be adjusted to fit other applications.

High-Pass Filters

The instrumentation amplifier in the AD8233 applies gain and high-pass filtering simultaneously. This capability allows the instrumentation amplifier to amplify a small ECG signal by 100 while rejecting electrode offsets as large as ±300 mV. The cutoff frequency of this filter is given by the following equation:

$$f_C = \frac{100}{2\pi \times R14 \times C7}$$

In this case, with R14 = 10 MΩ and C7 = 0.22 µF, place the pole of the first high-pass filter at 7 Hz. Note that the filter cutoff is 100 times higher than is typically expected because of the feedback architecture of the instrumentation amplifier (see Figure 4).

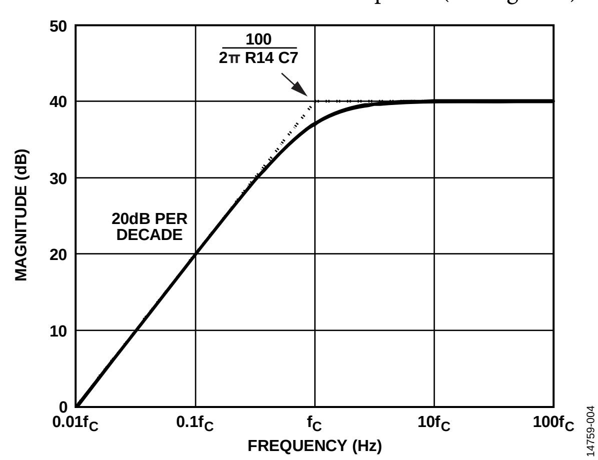

Figure 4. Frequency Response Instrumentation Amplifier Filter

An ac coupling network (C4 and R12) at the output of the instrumentation amplifier introduces a second pole. The cutoff frequency (f_C) is that of a regular passive first-order, high-pass filter and is shown in the following equation:

$$f_C = \frac{100}{2\pi \times R12 \times C4}$$

This results in a 7 Hz cutoff frequency for 0.22 µF and 100 kΩ. Both high-pass filters together yield a total roll-off of 40 dB per decade. Be aware that setting the same pole location for both high-pass filters results in 6 dB attenuation at the corner frequency. Because the output of this filter is unbuffered, the instrumentation amplifier exhibits higher output impedance at the input of the subsequent low-pass filter. The component values selected on the AD8233CB-EBZ evaluation board yield good results without a buffer. Keep this in mind when changing component values.

Low-Pass Filters

The internal uncommitted operational amplifier builds a two-pole low-pass filter with gain, using a Sallen-Key topology. The following design equations set the low-pass cutoff frequency, gain, and Q, respectively:

$$f_C = \frac{1}{2\pi\sqrt{R13 \times C8 \times R16 \times C9}}$$

$$Gain = 1 + \frac{R19}{R20}$$

$$Q = \sqrt{\frac{R13 \times C8 \times R16 \times C9}{R13 \times C9 + R16 \times C9 + R16 \times C8(1 - Gain)}}$$

Changing the gain or the cutoff frequency has an effect on Q, and vice versa.

The AD8233CB-EBZ evaluation board components place the cutoff frequency for the low-pass filter at approximately 25 Hz and the gain to 11. Keep the sum of R19 and R20 more than 50 kΩ to save power and avoid excessive loading of the output.

Figure 5 shows the transfer function of the signal from the differential input of the instrumentation amplifier to OUT with the default filter configuration.

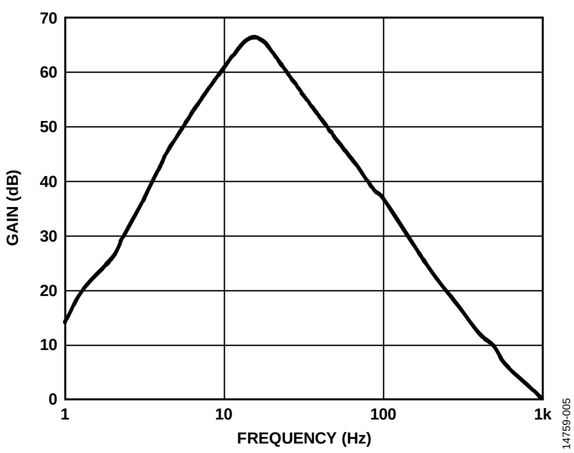

Figure 5. Gain vs. Frequency

Additional Low-Pass Filters

The R21, C14, R22, and C15 components offer additional filtering options. The OUTF terminal (TP16) is located after the first filter (R21 and C14). The OUTFF terminal (TP17) is located after both filters.

LEADS ON/OFF DETECTION

The AD8233 includes a leads on/off detection feature that remains functional in shutdown. It provides modes optimized for either two-electrode or three-electrode configurations for the device. Table 2 summarizes the different various configurations for leads on/off detection.

Table 2. Leads On/Off Detection Various Configurations

Configuration	Setting	Position
DC two-electrode leads on/off detection	Input Bias Selection	P4
	S2	DC
	S4	RLD_SDN
	Electrode Terminals	P2, P6
DC three-electrode leads on/off detection	Input Bias Selection	P4
	S2	DC
	S4	RLD_EN
	Electrode Terminals	P6, P7
AC two-electrode leads on/off detection	Input Bias Selection	P3 or P5
	S2	AC
	S4	RLD_SDN or RLD_EN
	Electrode Terminals	P6, P7
AC three-electrode leads on/off detection	Input Bias Selection	OPEN
	S2	AC
	S4	RLD_EN
	Electrode Terminals	OPEN

DC Leads On/Off Detection

The dc leads on/off detection mode can be used in two- or three-electrode configurations. To use this mode, place the S2 switch in the DC position. It works by sensing when either instrumentation amplifier input voltage is within 0.27 V from the positive rail. The lowest power consumption for the AD8233 is the two-electrode dc mode. A pull-up resistor on the +IN pin and a pull-down resistor on the–IN pin creates a voltage divider when the electrodes are connected, setting the input common mode to midsupply. To utilize these resistors on the AD8233CB-EBZ evaluation board, place a jumper at P6 and at P2. When the electrodes disconnect, the comparator monitoring the +IN pin sets the LOD pin high when the input pulls to the $+V_S$ pin. To create this connection, place a jumper at P4 (see Figure 6).

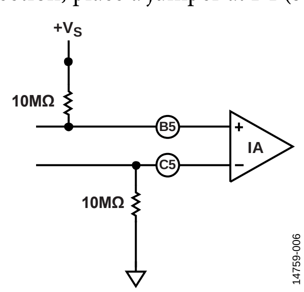

Figure 6. Circuit Configuration for Two-Electrode DC Leads Off Detection

For three-electrode dc mode, each input must have a pull-up resistor connected to the positive supply. During normal operation, the potential of the subject must be inside the common-mode range of the instrumentation amplifier, which is only possible if a third electrode is connected to the output of the RLD amplifier. To create this connection, place jumpers at P4, P6, and P7. RLD must also be enabled by putting the S4 switch in the RLD_EN position.

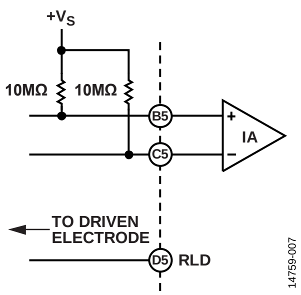

Figure 7. Circuit Configuration for Three-Electrode DC Leads Off Detection

The AD8233 indicates when any electrode is disconnected by setting the LOD pin high.

AC Leads On/Off Detection

The ac leads on/off detection mode is useful when using two-electrodes. To use the ac leads on/off mode, switch the S2 switch to the AC position. In this case, a conduction path must exist between the two-electrodes, which is usually formed by two resistors, shown in Figure 8.

These resistors also provide a path for bias return on each input. Connect each resistor (place jumpers at P6 and P7) to the REFOUT pin (place a jumper at P3) or RLD pin (place a jumper at P5) to maintain the inputs within the common-mode range of the instrumentation amplifier. If the resistors are tied to the RLD pin, the S4 switch must be in the RLD_EN position.

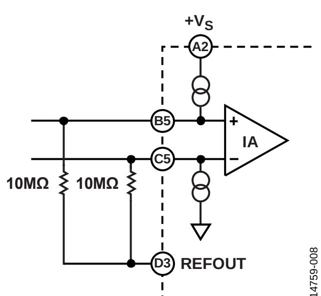

Figure 8. Circuit Configuration for Two-Electrode AC Leads Off Detection

The AD8233 detects when an electrode is disconnected by forcing a small 100 kHz current into the input terminals. This current flows through the external resistors from the +IN pin to the −IN pin and develops a differential voltage across the inputs, which is then synchronously detected and compared to an internal threshold. The recommended value for these external resistors is 10 MΩ. Low resistance values make the differential drop too low to be detected and lower the input impedance of the amplifier.

When the electrodes are attached to the subject, the impedance of this path must be less than 3 MΩ to maintain the drop below the comparator threshold.

While the REFOUT pin is at a constant voltage value, using the RLD output as the input bias may be more effective in rejecting common-mode interference at the expense of additional power.

In three-electrode ac leads off detection mode, shown in Figure 9, pull-up resistors are not required, which imporves the input impedance of the circuit. This mode is beneficial for dry electrode applications. The ac mode currents do contribute 1/f noise to the system; therefore, depending on the application, it can be advantageous to utilize ac leads off as a spot check and switches to dc mode for improved ECG acquisition. To create this connection, remove the Input Bias Selection jumpers and the Electrode Terminals jumpers.

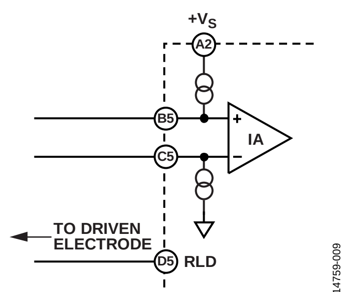

Figure 9. Circuit Configuration for Three-Electrode AC Leads Off Detection

The ac leads off detection mode continues to function in shutdown mode. To keep power under 1 µA, the clock is disabled and the ac currents become dc currents. The current source on the +IN pin is 250 nA, while the current sink on the −IN pin is −300 nA. The stronger pull-down current on −IN acts as a wake-up function, pulling the LOD pin low when the electrodes are reconnected.

FAST RESTORE

The fast restore function (FR) reduces the duration of otherwise long settling tails of the high-pass filters. After an abrupt change that rails the amplifier, such as a leads off condition, the AD8233 automatically adjusts to a higher filter cutoff frequency. This function allows the AD8233 to recover quickly and, therefore, take valid measurements soon after reconnecting the electrodes to the subject. To enable this function, set the S1 switch to the FR_EN position.

STANDBY OPERATION

The AD8233 includes a shutdown pin ($\overline{\text{SDN}}$) that further enhances the flexibility and ease of use in portable applications where power consumption is critical. To enter standby operation, place the S3 switch in the SDN position. In this condition, the AD8233 draws less than 1 µA of supply current, offering considerable power savings. To enter normal operation, place the S3 switch in the EN position.

During shutdown operation, the AD8233 is not able to maintain the REFOUT voltage, but it does not drain the REFIN voltage, thereby maintaining this additional conduction path from the supply to ground.

When emerging from a shutdown condition, the charge stored in the capacitors on the high-pass filters can saturate the instrumentation amplifier and subsequent stages. The use of the fast restore feature helps reduce the recovery time and, therefore, minimize time in power sensitive applications

EVALUATION BOARD COMPONENT SELECTION

Table 3. AD8233CB-EBZ Component Selection by Type

Reference Designator	Type	Description
P1, R24, R25, R26	3.5 mm electrode jack	Connect a sensor cable (not included) to the 3.5 mm electrode jack and connect the electrodes to a signal source such as an ECG signal generator. If not using the 3.5 mm electrode jack, remove R24, R25, and R26.
P3, P4, P5, R3, R4, R5	Input bias selection	Refer to the Leads On/Off Detection section for more information.
P2, P6, P7	Electrode terminals	Refer to the Leads On/Off Detection section for more information.
C7, R14	High-pass filter of the instrumentation amplifier	The cutoff frequency is set to 7.2 Hz. Refer to the High-Pass Filters section for more information.
C4, R12	AC-coupled filter	The cutoff frequency of this high-pass filter is set to 7.2 Hz. Because this is a dc blocking circuit, connecting R9 to the REFOUT voltage is necessary to allow negative signal swings. Refer to the High-Pass Filters section for more information.
R19, R20, R13, R16, C8, C9, C10	Low-pass filter (Sallen-Key)	This circuit provides two functions: a dual-pole, low-pass filter and gain. On the AD8233CB-EBZ evaluation board, the cutoff of this filter is set at 25 Hz and the gain to 11. This brings the total gain of the AD8233 to 11 × 100 = 1100. Refer to the Low-Pass Filters section for more information.
R21, R22, R23, C14, C15, C16	Additional low-pass filters	Not populated. These filters provide pads for the user to add additional filtering on the output and the reference voltage. Refer to the Additional Low-Pass Filters section for more information.
R17, R18, C11, P8, P9	REFIN resistor divider EN	R17 and R18 form a supply ratiometric reference voltage for the system. To utilize the ratiometric reference voltage, place jumpers at P8 and P9. The AD8233 buffers this voltage and makes it available at the REFOUT terminal. Select high resistor values for R17 and R18 to reduce power consumption. The AD8233CB-EBZ evaluation board uses 10 MΩ for both. C11 is required for filtering and stability. Power line noise may be considerably worse without C11. Due to the large resistor and capacitor values used on the AD8233CB-EBZ evaluation board, the time constant for this voltage is 5 sec and takes about 30 sec to observe a stable voltage at the output of REFOUT after power-up. Shutting down the AD8233 through S3 does not discharge C11 and there is no settling time related to this voltage.
C1, R2, R5, R8	Right leg drive	C1 is 1 nF, which, together with an internal 150 kΩ resistor, results in a loop gain of 20 around the typical line frequencies and a crossover frequency of 1 kHz. The value of R2 is set to 499 kΩ to avoid stability problems. For more information, refer to the Right Leg Drive (RLD) Amplifier section. R8 is not populated. It can limit the loop gain at low frequencies and shift the dominant pole of the amplifier.
R6, R7, C2, C3, C5	Optional RFI filter	Pads are provided for capacitors to implement additional radio frequency interference (RFI) filtering. C3 and C5 must be the same value and well matched. C2 must be a larger value than C3 and C5. This minimizes degradation of CMRR at higher frequencies from tolerance mismatch of C3 and C5. If C3 = C5 = C and R6 = R7 = R, the common mode signal cutoff frequency is $1/(2\pi RC)$ and the differential signal cutoff frequency is $1/(2\pi R(2 \times C2 + C))$. A lower common-mode signal cutoff frequency improves RFI rejection; however, it can increase the risk of instability with a right leg drive feedback loop. Thoroughly clean the AD8233CB-EBZ evaluation board after any rework. Leaving contaminants such as residual flux from soldering has a negative impact on the input impedance and operation of the AD8233CB-EBZ evaluation board.

EVALUATION BOARD SCHEMATIC AND ARTWORK

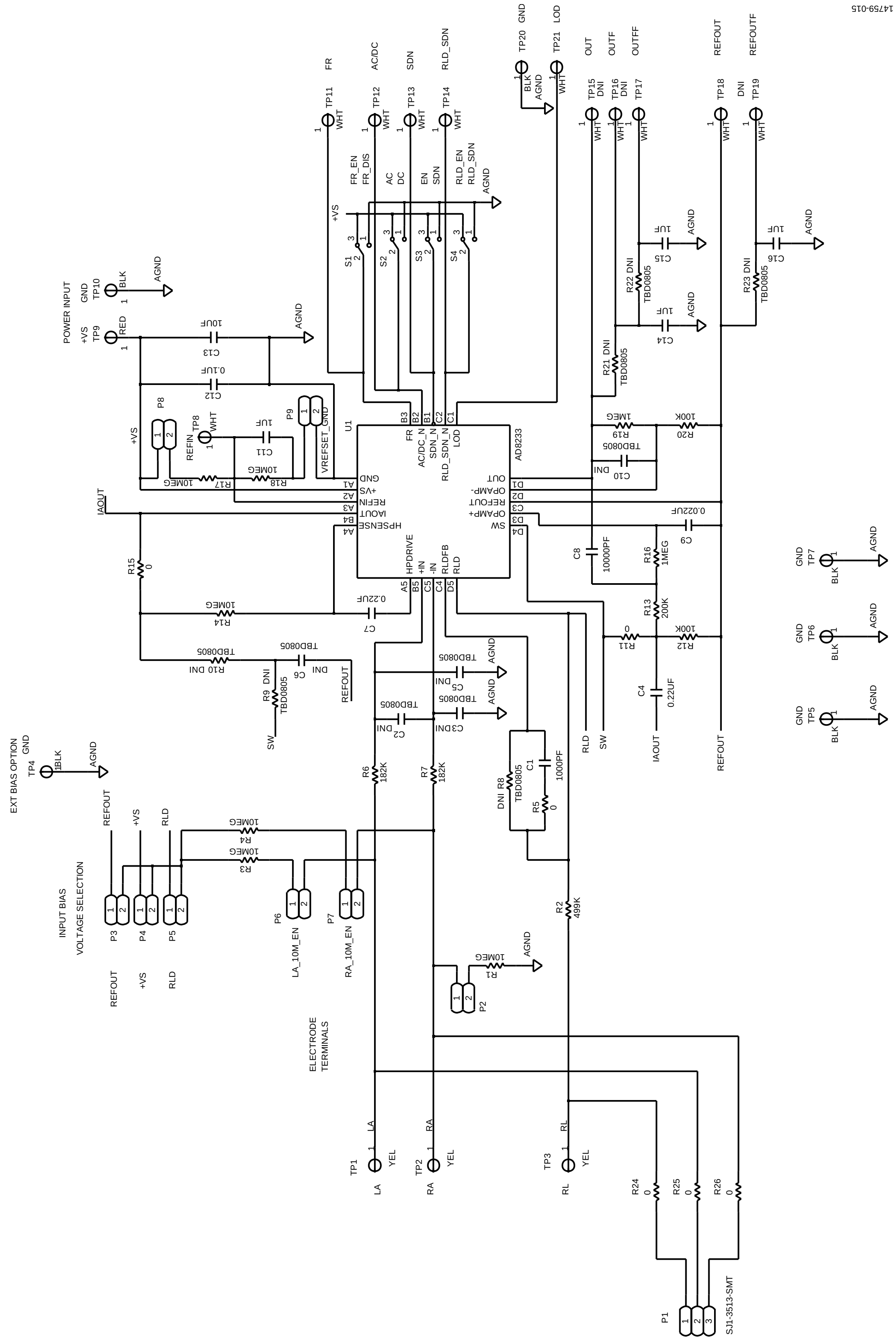

Figure 10. AD8233CB-EBZ Schematic

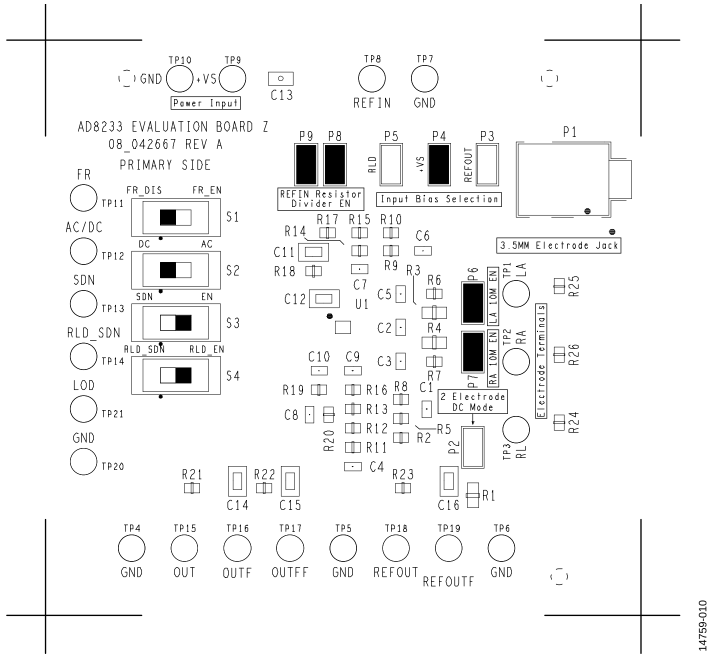

Figure 11. AD8233CB-EBZ Evaluation Board Top Assembly

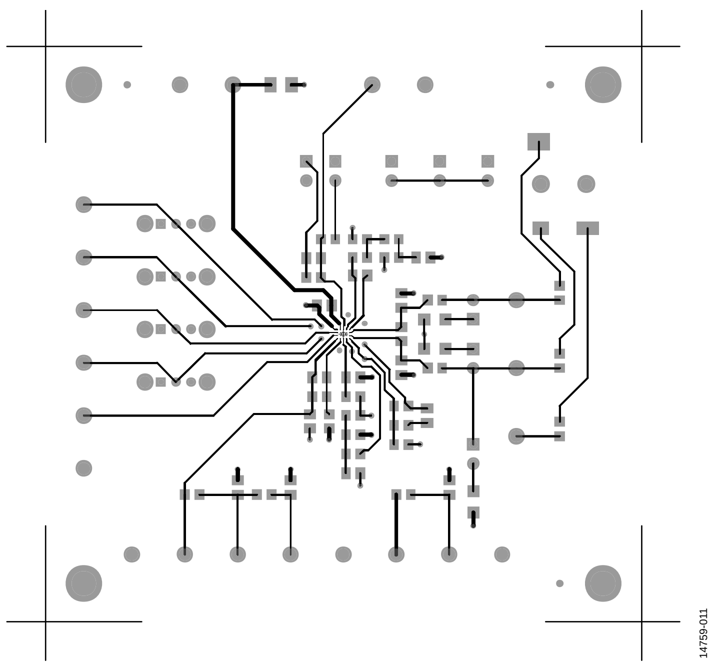

Figure 12. AD8233CB-EBZ Evaluation Board Primary Side, Copper

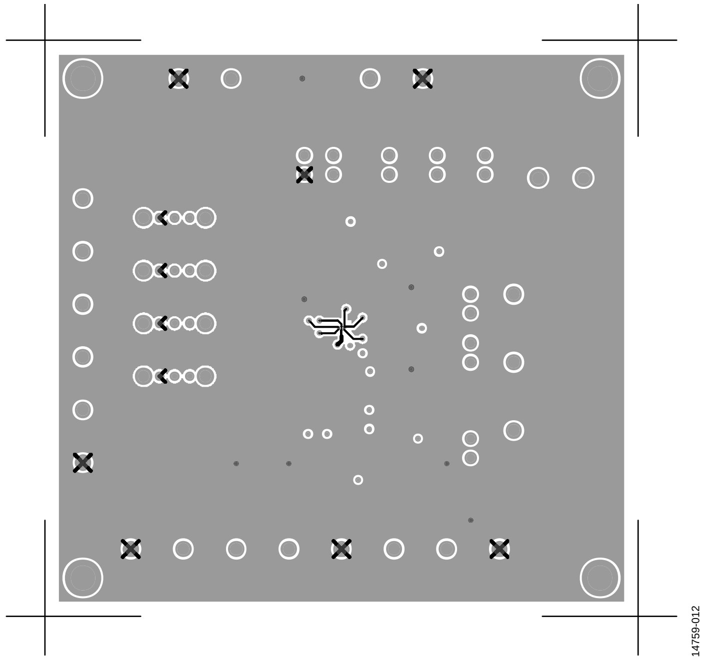

Figure 13. AD8233CB-EBZ Evaluation Board Layer 2, Copper

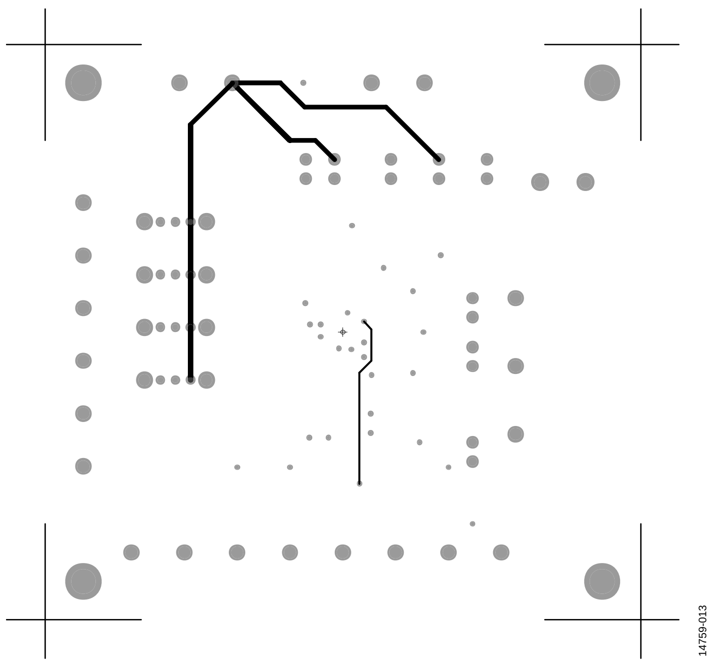

Figure 14. AD8233CB-EBZ Evaluation Board Layer 3, Copper

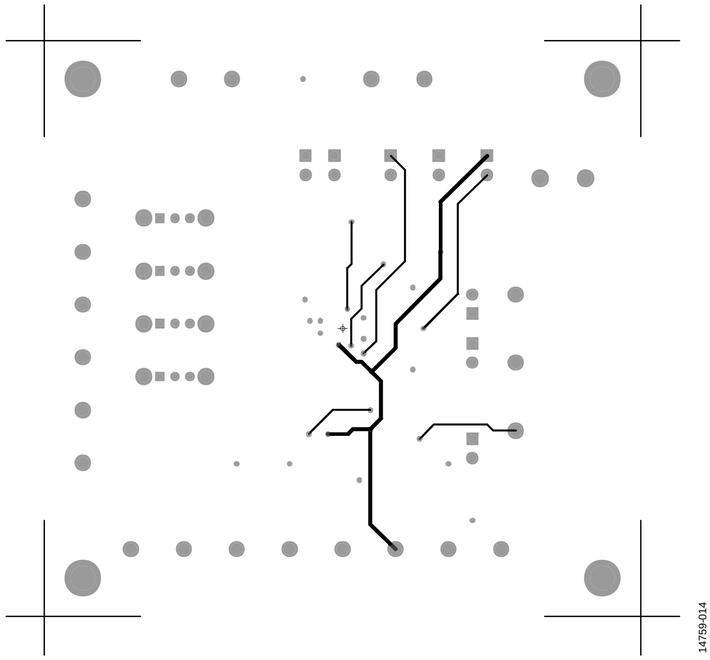

Figure 15. AD8233CB-EBZ Evaluation Board Secondary Side, Copper

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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