Low Input Voltage, Synchronous Step-Down DC/DC Controller

FEATURES

- **Charge Pump Input Range: 2.7V to 5.5V**
- **Controller Input Range: 4V to 38V**
- **Integrated Charge Pump Provides 5V Gate Drive to Logic Level MOSFETs**
- **R_{SENSE} or DCR Current Sensing**
- **±1.25% Output Voltage Accuracy Over Temperature**
- **Phase-Lockable Fixed Frequency: 250kHz to 750kHz**
- Power Good Output Voltage Monitor
- Adjustable Soft-Start Voltage Ramping
- Current Foldback Disabled During Start-Up
- No Reverse Current During Soft-Start
- Selectable Constant Frequency, Pulse-Skipping, or Burst Mode Operation
- Output Overvoltage Protection
- Very Low Dropout Operation: 99% Duty Cycle
- Available in a 24-Lead (3mm × 5mm) QFN Package

APPLICATIONS

- General Purpose 3.3V Systems
- Lithium-Ion Powered Devices
- Distributed DC Power Systems

DESCRIPTION

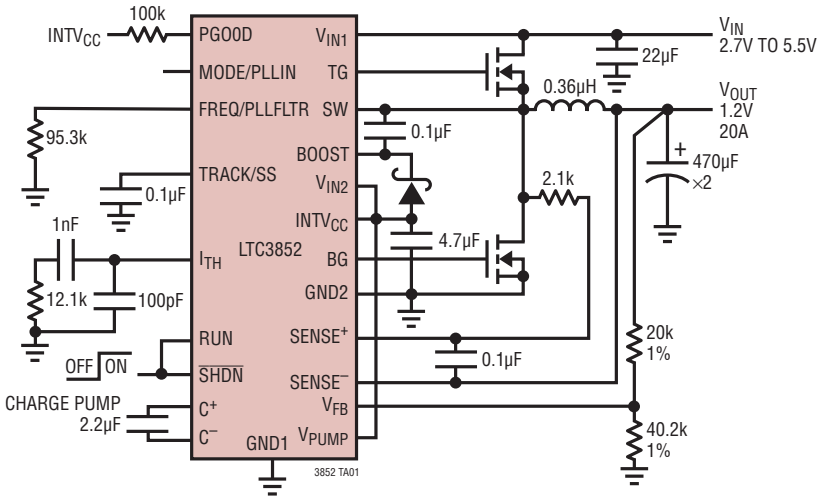
The LTC®3852 is a constant frequency, current mode step-down DC/DC controller which can be powered by an onboard charge pump. Input supplies as low as 2.7V, when doubled by the charge pump, provide 5V to the LTC3852's control logic and gate drives, supporting a wide selection of logic-level N-channel power MOSFETs.

The constant-frequency current mode architecture allows for a phase-lockable fixed frequency of up to 750kHz. The RUN pin provides a precision enable threshold while the TRACK/SS pin combines tracking and adjustable soft-start features.

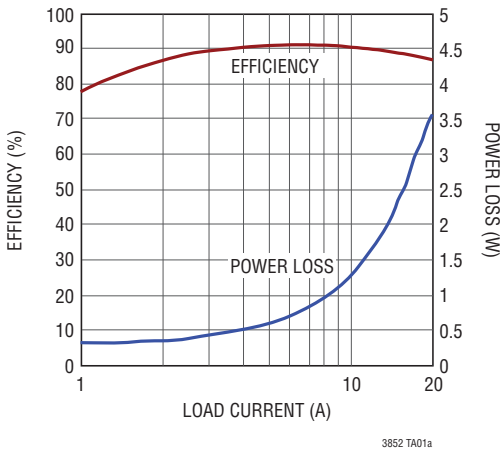
The MODE/PLLIN pin selects among Burst Mode® operation, pulse-skipping mode, and continuous current mode. Current foldback limits MOSFET power dissipation during short-circuit conditions. Reverse current and current foldback functions are disabled during soft-start. A power good output pin indicates when the output is within ±10% of its designed set point.

TYPICAL APPLICATION

High Efficiency Synchronous Step-Down Converter



Efficiency and Power Loss vs Load Current

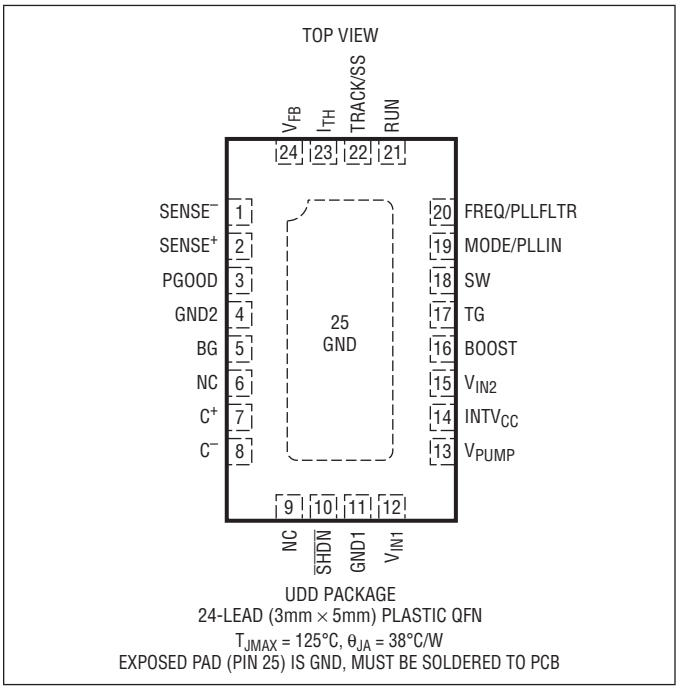


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN1}) ..... 6V to –0.3V
Top Side Driver Voltage (BOOST)..... 46V to –0.3V
Switch Voltage (SW)..... 40V to –0.3V
V_{PUMP} ..... 5.5V to –0.3V
$\overline{SHDN}$, RUN..... 6V to –0.3V
V_{PUMP} Short-Circuit Duration ..... Indefinite
V_{IN2}..... 40V to –0.3V
$INTV_{CC}$, (BOOST-SW), RUN, PGOOD ..... 6V to –0.3V
$INTV_{CC}$, Peak Output Current..... 50mA
$SENSE^+$, $SENSE^-$..... 6V to –0.3V
MODE/PLLIN, TRACK/SS ..... $INTV_{CC}$ to –0.3V
FREQ/PLLFLTR ..... $INTV_{CC}$ to –0.3V
I_{TH}, V_{FB} ..... 3V to –0.3V
Operating Junction Temperature (Note 2)..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3852EUDD#PBF	LTC3852EUDD#TRPBF	LFRJ	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3852IUDD#PBF	LTC3852IUDD#TRPBF	LFRJ	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN1} = 3.3V, V_{IN2} = 15V, V_{RUN} = 3.3V, $\overline{SHDN}$ = 0V, MODE/PLLIN = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop (Step-Down Regulator)							
V_{IN2}	Controller Input Voltage Range		●	4		38	V
V_{FB}	Regulated Feedback Voltage	(Note 3); I_{TH} Voltage = 1.2V	●	0.790	0.800	0.810	V
I_{FB}	Feedback Current	(Note 3)			–10	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Notes 3, 9); V_{IN2} = 6V to 38V			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 1.6V	●		–0.01	–0.1	%
g_m	Transconductance Amplifier g_m	(Note 3); I_{TH} = 1.2V; Sink/Source 5µA			2		mmho
$I_{Q(VIN2)}$	Controller Input DC Supply Current	(Note 4) V_{FB} = 0.9V (RUN = 3.3V)			1.4		mA
	Shutdown Supply Current	RUN = 0V			25	50	µA
$I_{Q(VIN1)}$	Total Input DC Supply Current	(Notes 4, 7) V_{FB} = 0.9V (RUN = $\overline{SHDN}$ = 3.3V)			7		mA
	Shutdown Supply Current	(Note 7) RUN = $\overline{SHDN}$ = 0V			5		µA
UVLO	Undervoltage Lockout	$INTV_{CC}$ Ramping Down			3.25		V
	Undervoltage Hysteresis				0.4		V
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{FB}	●	0.86	0.88	0.90	V
I_{SENSE}	SENSE Pins Current			–2.0		2.0	µA
$I_{TRACK/SS}$	Soft-Start Charge Current	$V_{TRACK/SS}$ = 0V		0.5	1	2	µA
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	●	1.1	1.22	1.35	V
$V_{RUN(HYS)}$	RUN Pin On Hysteresis				130		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V, V_{SENSE}^- = 3.3V	●	40	53	68	mV
TG R_{UP}	TG Driver Pull-Up On-Resistance	TG High			2.2		Ω
TG R_{DOWN}	TG Driver Pull-Down On-Resistance	TG Low			1.2		Ω
BG R_{UP}	BG Driver Pull-Up On-Resistance	BG High			2.1		Ω
BG R_{DOWN}	BG Driver Pull-Down On-Resistance	BG Low			1.1		Ω
TG t_r TG t_f	Top Gate Rise Time Top Gate Fall Time	C_{LOAD} = 3300pF (Note 5)			25 25		ns ns
BG t_r BG t_f	Bottom Gate Rise Time Bottom Gate Fall Time	C_{LOAD} = 3300pF (Note 5)			25 25		ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF (Note 5)			30		ns
BG/TG t_{1D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF (Note 5)			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 6)			90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN1} = 3.3V, V_{IN2} = 15V, V_{RUN} = 3.3V, $\overline{SHDN}$ = 0V, MODE/PLLIN = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop (Step-Down Regulator)							
f_{NOM1}	Nominal Frequency	R_{FREQ} = 60k		460	500	540	kHz
f_{LOW1}	Lowest Frequency	R_{FREQ} = 160k		205	235	265	kHz
f_{HIGH1}	Highest Frequency	R_{FREQ} = 36k		690	750	810	kHz
f_{NOM2}	Nominal Frequency	R_{FREQ} = 60k (Note 7)		460	500	540	kHz
f_{LOW2}	Lowest Frequency	R_{FREQ} = 160k (Note 7)		205	235	265	kHz
f_{HIGH2}	Highest Frequency	R_{FREQ} = 36k (Note 7)		690	750	810	kHz
f_{MODE}	MODE/PLLIN Minimum Input Frequency MODE/PLLIN Maximum Input Frequency	MODE/PLLIN = External Clock			250 750		kHz kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				100		kΩ
I_{FREQ}	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{MODE} > f_{OSC}$ $f_{MODE} < f_{OSC}$			 –90 75		 µA µA
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Regulated Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive		 –12 8	 –10 10	 –8 12	 % %
V_{PUMP} Charge Pump Supply (V_{IN1} = 3.3V; $V_{\overline{SHDN}}$ = 3.3V, V_{RUN} = 0); C_{VIN1} = 4.7µF, C_{FLY} = 2.2µF, C_{VPUMP} = 4.7µF							
V_{IN1}	Input Voltage Range			2.7		5.5	V
V_{PUMP}	Charge Pump Doubler Output Voltage	C_{FLY} = 2.2µF 2.7V < V_{IN1} < 5.5V; I_{VPUMP} = 1mA	●	4.8	5.05	5.3	V
$I_{\overline{SHDN}}$	Shutdown Pin Current	$\overline{SHDN}$ = 0V; V_{PUMP} = 0V				1	µA
V_{RIPPLE}	Output Ripple at V_{PUMP}	I_{VPUMP} = 50mA (Note 10)			20		mV_{P-P}
f_{PUMP}	Charge Pump Frequency			0.6	1.2	1.8	MHz
V_{IH}	$\overline{SHDN}$ Input Threshold		●	1.3			V
V_{IL}	$\overline{SHDN}$ Input Threshold		●			0.4	V
I_{IH}	$\overline{SHDN}$ Input Current			–1		1	µA
I_{IL}	$\overline{SHDN}$ Input Current			–1		1	µA
R_{OL}	Effective Open-Loop Output Resistance (Note 8)	V_{IN1} = 2.7V, V_{PUMP} = 4.5V			6		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3852 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3852E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3852I is guaranteed over the –40°C to 125°C operating junction temperature range. T_J is calculated from the ambient temperature, T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet 38°C/W)$$

Note 3: The LTC3852 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications information.

Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels. Rise and fall times are assured by design, characterization and correlation with statistical process controls.

Note 6: The minimum on-time condition is specified for an inductor peak-to-peak ripple current equal to 40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information Section).

Note 7: V_{IN1} = 3.3V; Connect V_{PUMP}, V_{IN2} and $INTV_{CC}$ together.

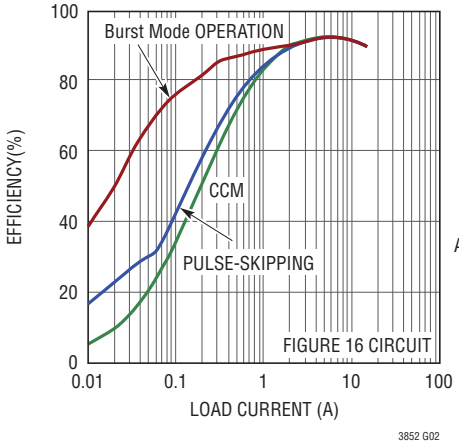
Note 8: $R_{OL} = (2V_{IN} - V_{OUT})/I_{OUT}$

Note 9: V_{IN2} swept while not connected to V_{PUMP} or $INTV_{CC}$.

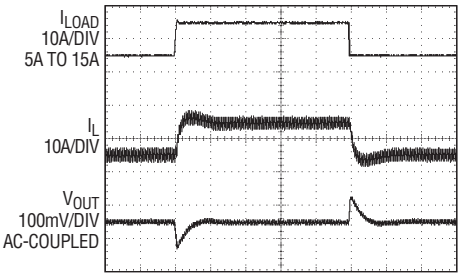
Note 10: Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Output Current and Mode

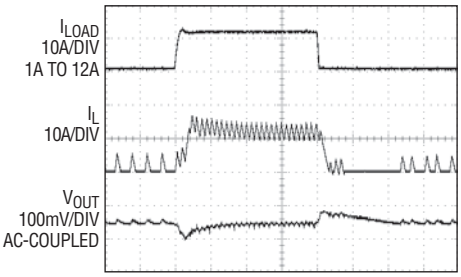


Load Step



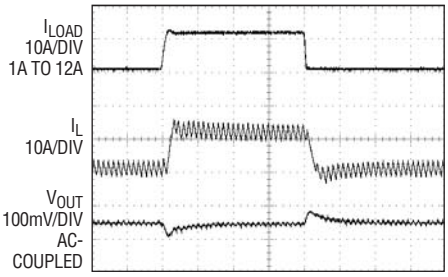
V_{OUT} = 1.5V 50µs/DIV
V_{IN1} = 3.3V
FIGURE 16 CIRCUIT

Load Step (Burst Mode Operation)



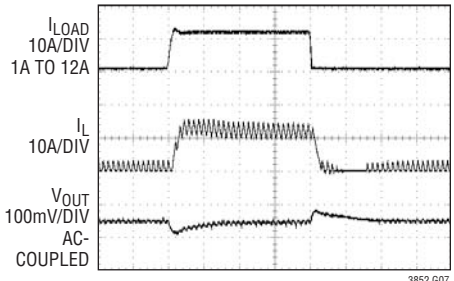
V_{OUT} = 1.2V 20µs/DIV
V_{IN1} = 3.3V
FIGURE 17 CIRCUIT

Load Step (Forced Continuous Mode)



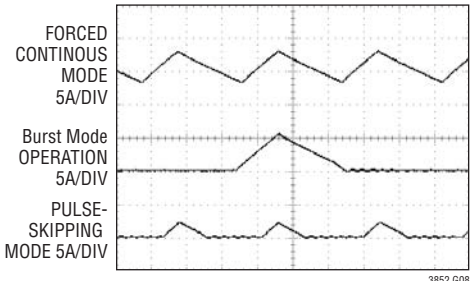
V_{OUT} = 1.2V 20µs/DIV
V_{IN1} = 3.3V
FIGURE 17 CIRCUIT

Load Step (Pulse-Skipping Mode)



V_{OUT} = 1.2V 20µs/DIV
V_{IN1} = 3.3V
FIGURE 17 CIRCUIT

Inductor Current at Light Load



V_{OUT} = 1.5V 1µs/DIV
V_{IN2} = 3.3V
I_{LOAD} = 500mA
FIGURE 17 CIRCUIT

Start-Up with Prebiased Output at 0.5V

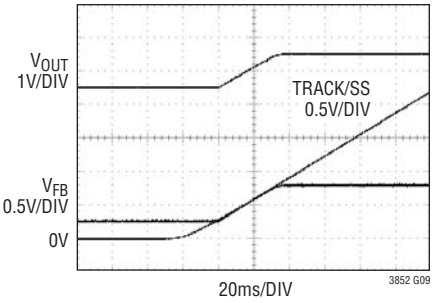


FIGURE 16 CIRCUIT

Coincident Tracking with Master Supply

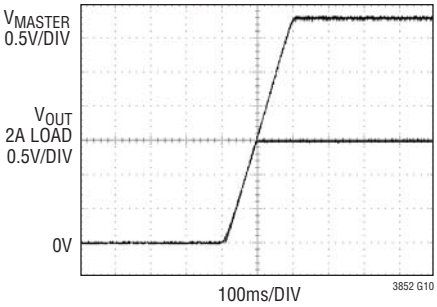


FIGURE 16 CIRCUIT

Ratiometric Tracking with Master Supply

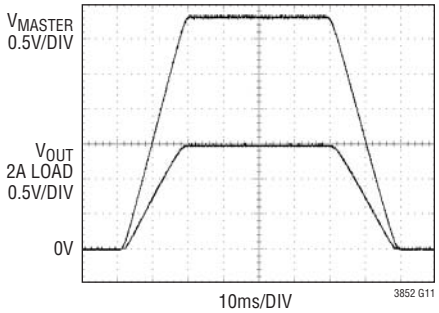
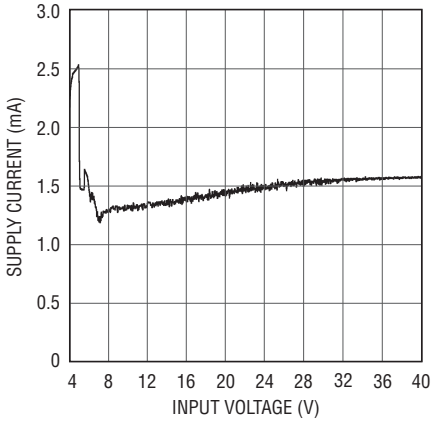


FIGURE 16 CIRCUIT

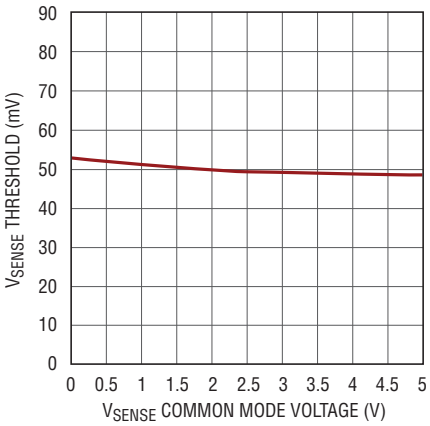
TYPICAL PERFORMANCE CHARACTERISTICS

Controller Input DC Supply Current vs Input Voltage (V_{IN2})



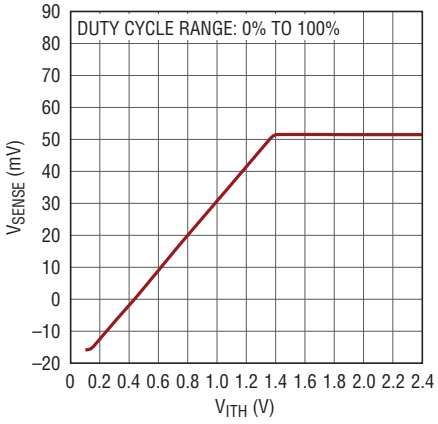
3852 G12

Controller Maximum Current Sense Threshold vs Common Mode Voltage



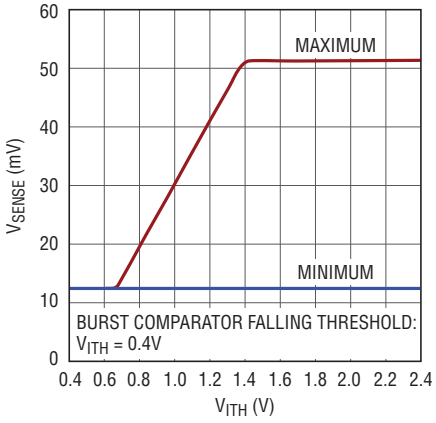
3852 G14

Controller Maximum Peak Current Sense Threshold vs I_{TH} Voltage



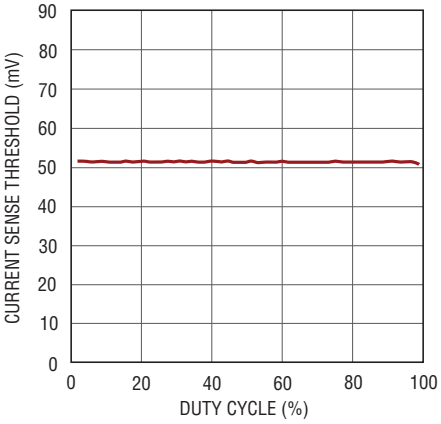
3852 G15

Controller Burst Mode Peak Current Sense Threshold vs I_{TH} Voltage



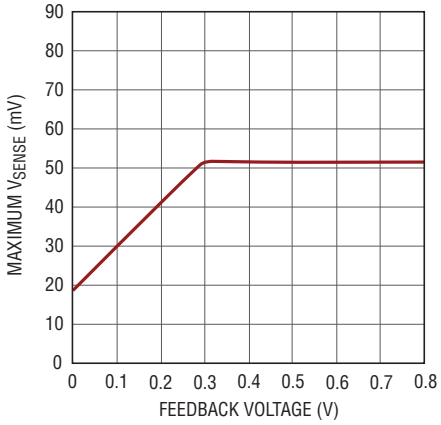
3852 G16

Controller Maximum Current Sense Threshold vs Duty Cycle



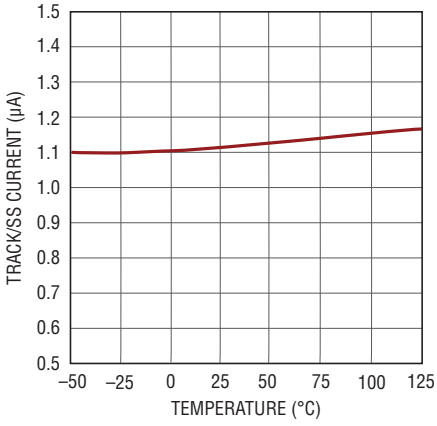
3852 G17

Controller Maximum Current Sense Threshold vs Feedback Voltage (Current Foldback)



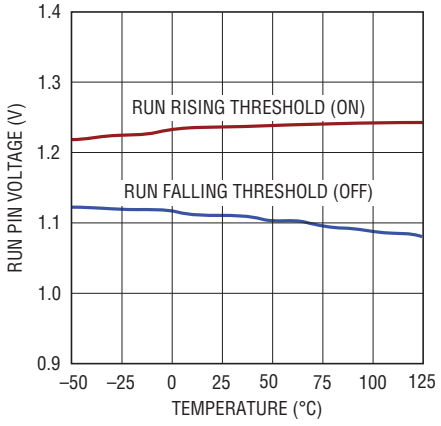
3852 G18

Controller TRACK/SS Pull-Up Current vs Temperature



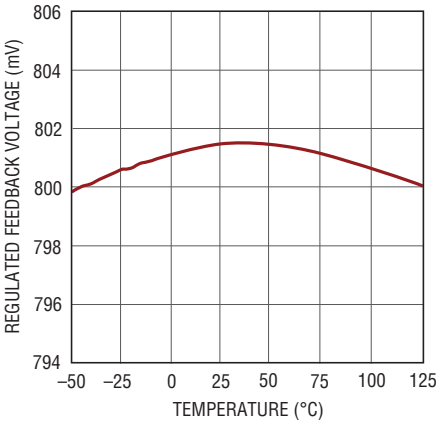
3852 G19

Controller Shutdown (RUN) Threshold vs Temperature



3852 G20

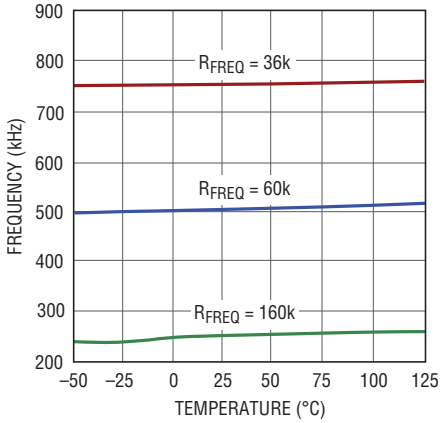
Controller Regulated Feedback Voltage vs Temperature



3852 G21

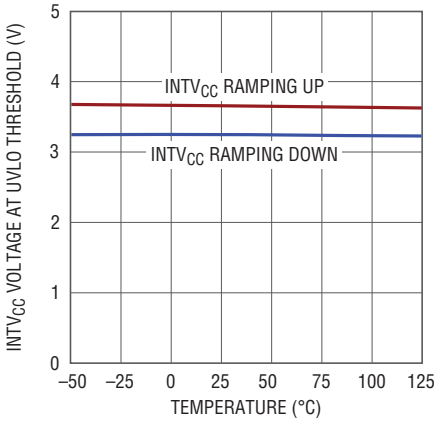
TYPICAL PERFORMANCE CHARACTERISTICS

Controller Oscillator Frequency vs Temperature



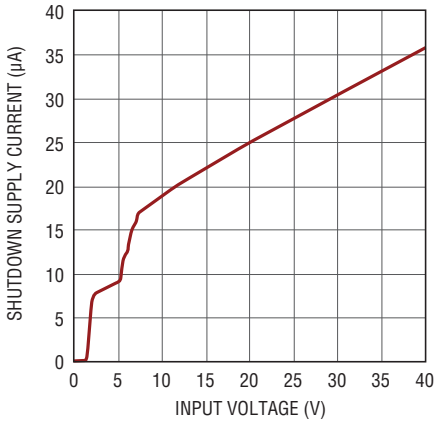
3852 G22

Controller Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



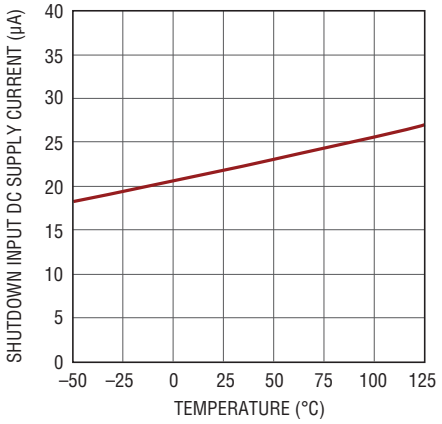
3852 G24

Shutdown Input DC Supply Current vs Input Voltage Controller Only



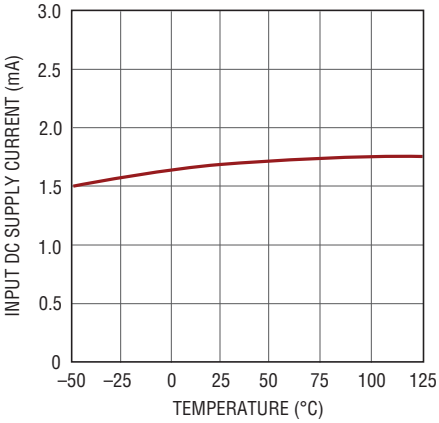
3852 G25

Shutdown Input DC Supply Current vs Temperature Controller Only



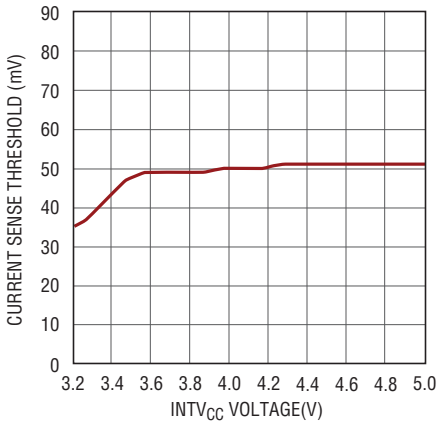
3852 G26

Input DC Supply Current vs Temperature Controller Only



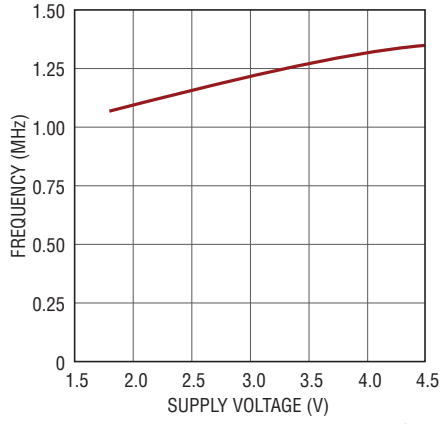
3852 G27

Maximum Current Sense Threshold vs $INTV_{CC}$ Voltage



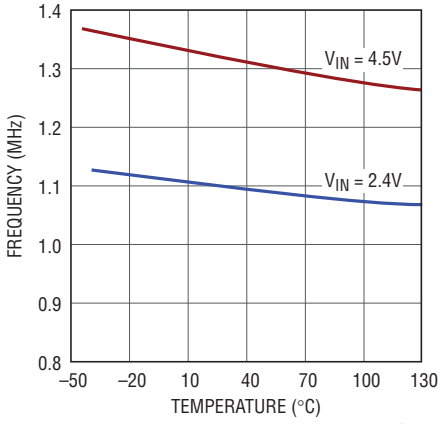
3852 G28

Charge Pump Oscillator Frequency vs Supply Voltage



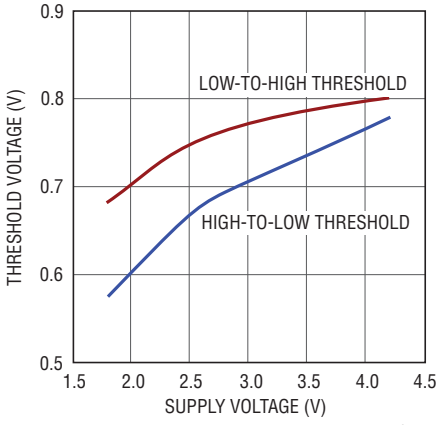
3852 G29

Charge Pump Oscillator Frequency vs Temperature



3852 G30

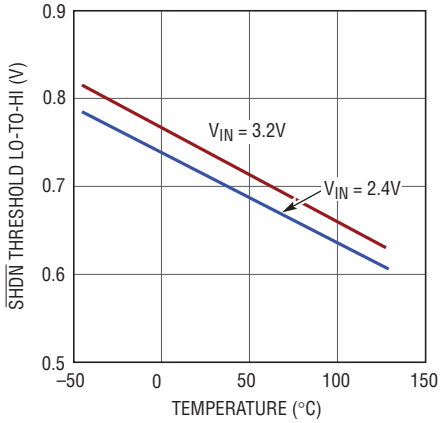
Charge Pump $\overline{SHDN}$ Threshold Voltage vs Supply Voltage



3852 G31

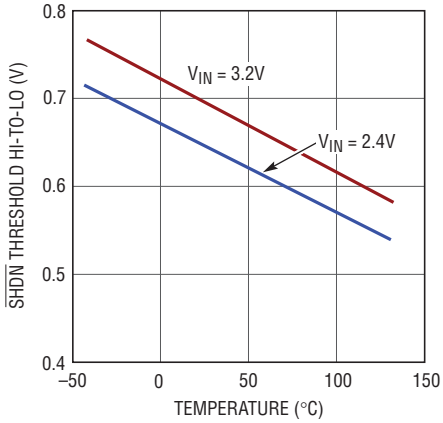
TYPICAL PERFORMANCE CHARACTERISTICS

Charge Pump
$\overline{SHDN}$ LO-to-HI Threshold
vs Temperature



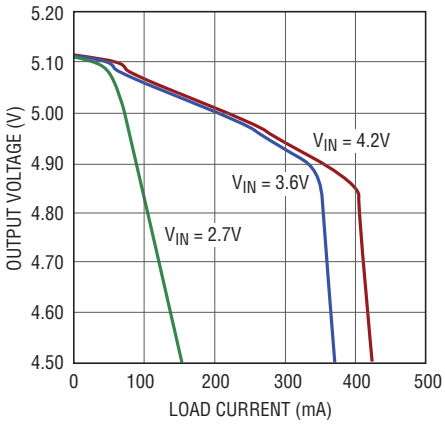
3852 G32

Charge Pump
$\overline{SHDN}$ HI-to-LO Threshold
vs Temperature



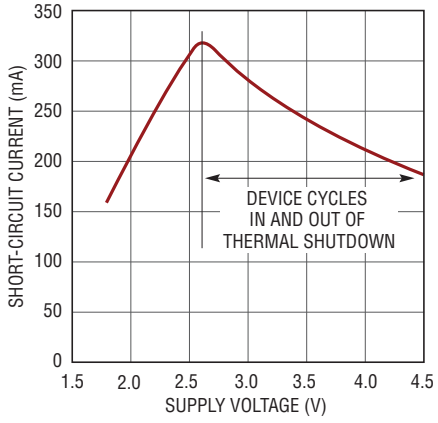
3852 G33

Charge Pump Load Regulation



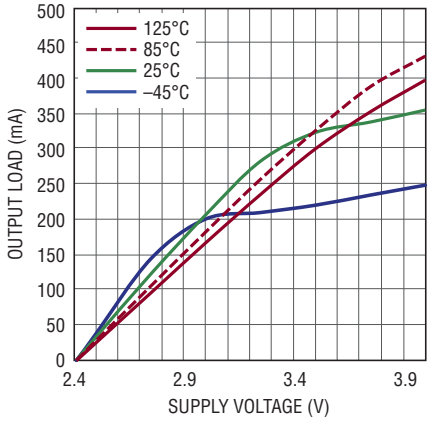
3852 G35

Charge Pump Short-Circuit
Current vs Supply Voltage



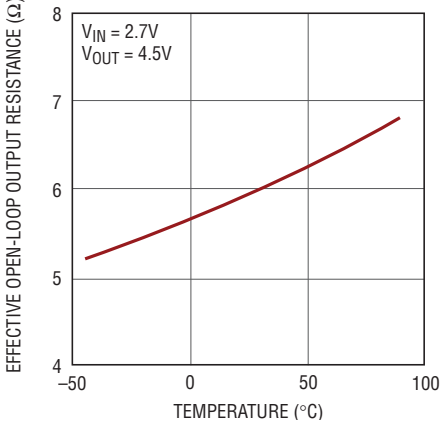
3852 G34

Charge Pump Output Load
Capability at 4% Below Regulation



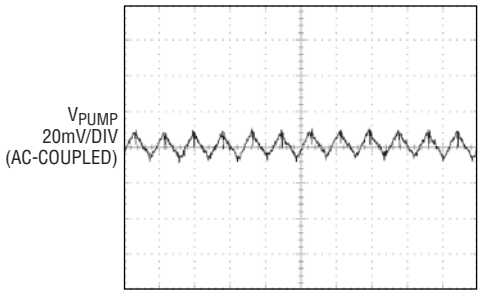
3852 G36

Charge Pump Effective Open-Loop
Output Resistance vs Temperature



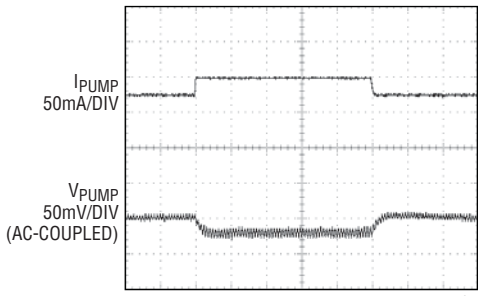
TYPICAL PERFORMANCE CHARACTERISTICS

Charge Pump Output Ripple



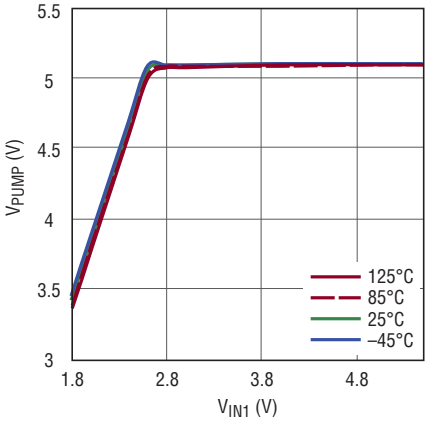
V_{IN1} = 3.3V 1µs/DIV
I_{PUMP} = 25mA
C_{VPUMP} = 4.7µF

Charge Pump Load Transient Response

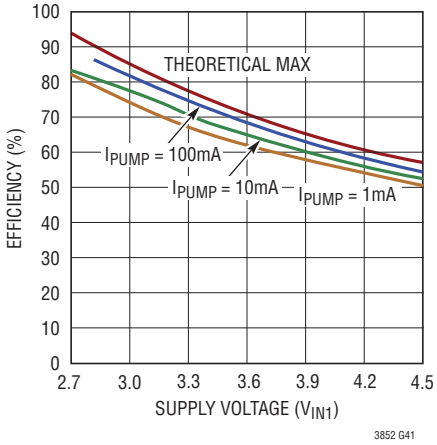


V_{IN} = 3.3V 10µs/DIV
I_{PUMP} = 25mA TO 50mA STEP

Charge Pump Line Regulation with 25mA Load



Efficiency vs Supply Voltage



PIN FUNCTIONS

SENSE⁻ (Pin 1): The (–) Input to the Current Sense Comparators. Kelvin connect to V_{OUT} at the current sense resistor or, if DCR sensing is used, at the inductor.

SENSE⁺ (Pin 2): Current Sense Comparator Noninverting Input. The (+) input to the current comparator is normally connected to the DCR sensing network or current sensing resistor.

PGOOD (Pin 3): Power Good Indicator Output. Open drain logic out that is pulled to ground when the output voltage exceeds the ±10% regulation window, after the internal 17µs power bad mask timer expires.

GND2 (Pin 4): Buck Controller Ground. All small-signal components and compensation components should be Kelvin connected to this ground. The (–) terminal of C_{INTVCC} should be closely connected to this pin. The exposed pad must be soldered to the PCB to provide electrical contact for the IC and for optimum thermal performance.

BG (Pin 5): Bottom Gate Driver Output. This pin drives the gate of the bottom N-channel MOSFET between GND and $INTV_{CC}$.

C⁺ (Pin 7): Flying Capacitor Positive Terminal.

PIN FUNCTIONS

C^- (Pin 8): Flying Capacitor Negative Terminal.

$\overline{SHDN}$ (Pin 10): Active Low Shutdown Input. A low on $\overline{SHDN}$ disables the charge pump. This pin must not be allowed to float.

GND1 (Pin 11): Charge Pump Ground. The (–) terminals of C_{IN} and C_{VPUMP} should be closely connected to this pin.

V_{IN1} (Pin 12): Input Supply Voltage to Charge Pump. V_{IN1} should be bypassed with a 1µF to 4.7µF low ESR ceramic capacitor.

V_{PUMP} (Pin 13): Regulated Output Voltage from Charge Pump. For best performance, V_{PUMP} should be bypassed with a low ESR ceramic capacitor providing at least 2.2µF of capacitance as close to the pin as possible.

$INTV_{CC}$ (Pin 14): Gate Drive Supply. The MOSFET drivers and internal logic are powered from this voltage. Bypass this pin to GND with a minimum 2.2µF low ESR tantalum or ceramic capacitor, C_{INTVCC}.

V_{IN2} (Pin 15): Main Supply Pin for Step-Down Controller. A bypass capacitor should be tied between this pin and the GND2 pin.

BOOST (Pin 16): Boosted Floating Driver Supply. The (+) terminal of the booststrap capacitor is connected to this pin. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN1} + $INTV_{CC}$.

TG (Pin 17): Top Gate Driver Output. This is the output of a floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage.

SW (Pin 18): Switch Node Connection to the Inductor. Voltage swing at this pin is from a diode (external) voltage drop below ground to the buck regulator power stage V_{IN}.

MODE/PLLIN (Pin 19): Forced Continuous Mode, Burst Mode operation or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to $INTV_{CC}$ to force continuous conduction mode of operation. Connect to GND2 to enable pulse-skipping mode of operation. To select Burst Mode operation, tie this pin to $INTV_{CC}$ through a resistor no less than 50k, but no greater than 250k. A clock on the pin will force the controller into forced continuous mode of operation and synchronize the internal oscillator.

FREQ/PLLFLTR (Pin 20): The phase-locked loop's lowpass filter is tied to this pin. Alternatively, a resistor can be connected between this pin and GND2 to vary the frequency of the internal oscillator.

RUN (Pin 21): Run Control Input. Forcing the pin below 1.25V shuts down the step-down controller. There is a 2µA pull-up current on this pin.

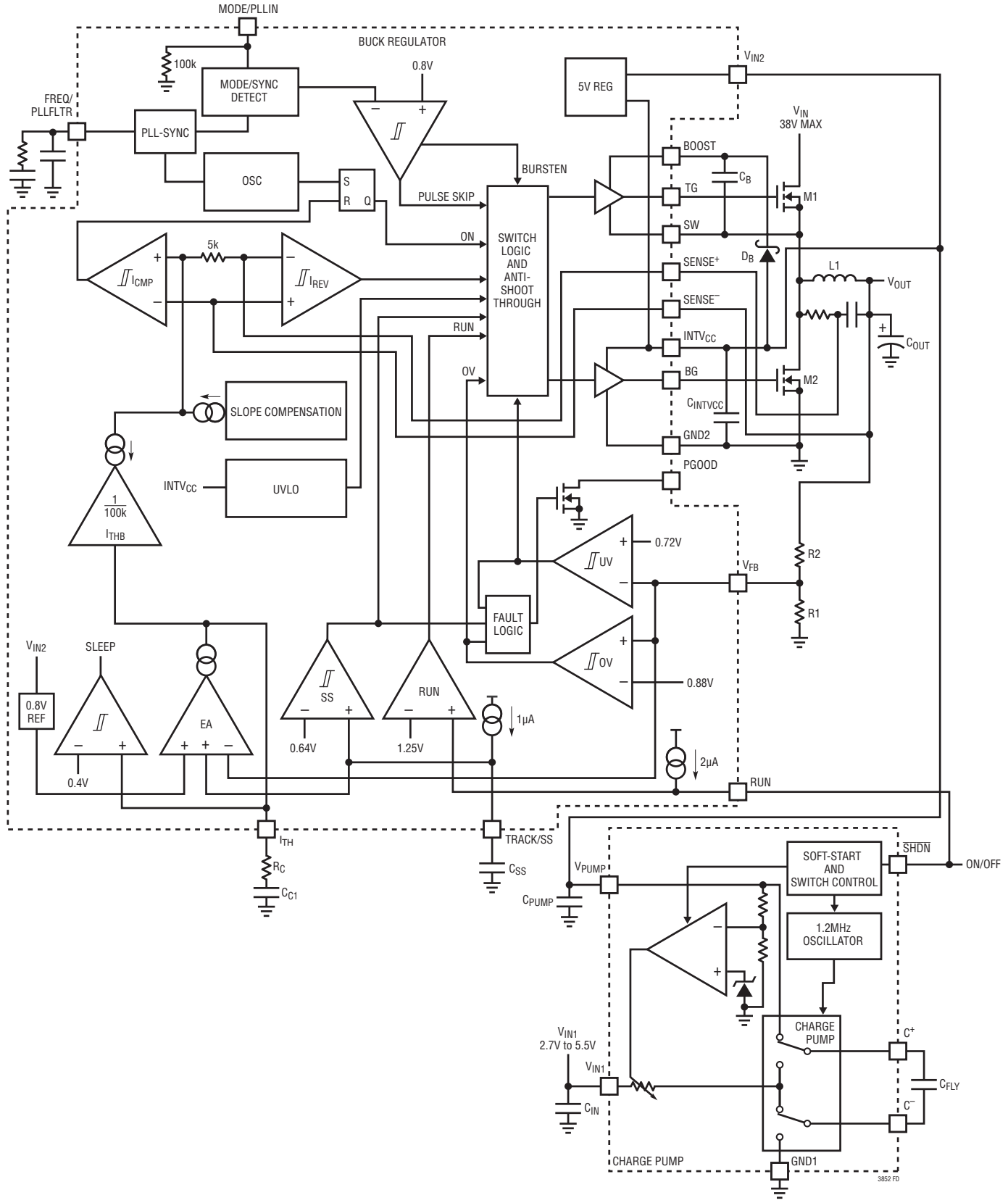
TRACK/SS (Pin 22): Output Voltage Tracking and Soft-Start Input. A capacitor to ground at this pin sets the ramp rate for the output voltage. An internal soft-start current of 1µA charges this capacitor.

I_{TH} (Pin 23): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator input threshold increases with this control voltage.

V_{FB} (Pin 24): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider across the output.

GND (Exposed Pad Pin 25): Ground. Must be soldered to PCB, providing a local ground for the IC.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3852 is a constant frequency, current mode step-down DC/DC controller which can be powered by an onboard charge pump. Supplies as low as 2.7V, when doubled by the charge pump, provide 5V to the LTC3852's control logic and gate drives, supporting a wide selection of logic-level MOSFETs.

During normal operation, the controller's top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator, I_{REV}, or the beginning of the next cycle.

The charge pump section uses a switched capacitor doubler to boost V_{IN1} to $2 \times V_{IN1}$, with a regulated maximum of 5V. Regulation is achieved by sensing the output voltage through an internal resistor divider and modulating the charge pump output current based on the error signal. A 2-phase nonoverlapping clock activates the charge pump switches. The flying capacitor is charged from V_{IN1} on the first phase of the clock. On the second phase of the clock it is stacked in series with V_{IN1} and connected to V_{PUMP}. This sequence of charging and discharging the flying capacitor continues at a free running frequency of 1.2MHz (typ).

Two configurations address most LTC3852 applications. Figure 1a covers the single low input voltage case, typically 3.3V. The input to the charge pump, V_{IN1}, is connected to the same input voltage as the drain of the top MOSFET. V_{PUMP}, V_{IN2} and $INTV_{CC}$ are tied together, so that the charge pump's 5V output provides all power to the buck controller section.

The alternative arrangement in Figure 1b allows the LTC3852 to step down from as high as 38V, while powering itself from an available 3.3V bus. The input to the charge pump, V_{IN1}, is connected to 3.3V instead of the drain of the top MOSFET. It is not necessary to step the high input voltage down to 5V through a linear regulator. Logic level MOSFETs are usable in both cases.

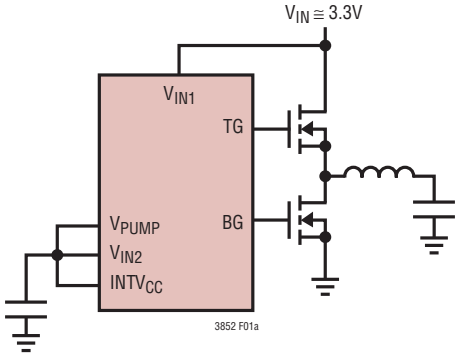


Figure 1a

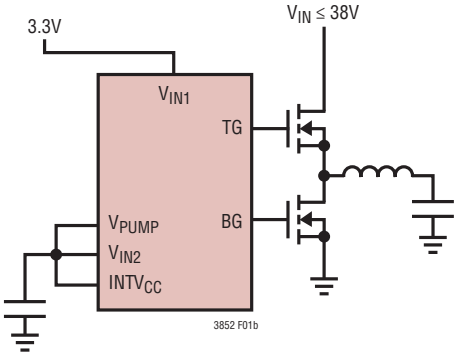


Figure 1b

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. Peak current drawn from $INTV_{CC}$ should not exceed 50mA.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 1/10 of the clock period every tenth cycle to allow C_B to recharge. However, it

OPERATION

is recommended that there is always a load present during the drop-out transition to ensure C_B is recharged.

Shutdown and Start-Up (RUN, $\overline{SHDN}$ and TRACK/SS)

The switching regulator section of the LTC3852 can be shut down using the RUN pin. Pulling this pin below 1.1V disables the controller and most of the internal circuitry. Releasing the RUN pin allows an internal 2µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin.

The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the LTC3852 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to GND. An internal 1µA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively, the TRACK/SS pin can be used to cause the start-up of V_{OUT} to "track" another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the RUN pin is pulled low to disable the controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.2V, the TRACK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

The charge pump is separately controlled by $\overline{SHDN}$. In shutdown mode, all charge pump circuitry is turned off and it draws only leakage current from the V_{IN1} supply. Furthermore, V_{PUMP} is disconnected from V_{IN1}. The $\overline{SHDN}$ pin is a CMOS input with a threshold voltage of approximately 0.7V. The charge pump is in shutdown when a logic low is applied to the $\overline{SHDN}$ pin. Since the $\overline{SHDN}$ pin is a very high impedance CMOS input, it should never be allowed to float. To ensure that its state is defined, it must always be driven with a valid logic level not exceeding V_{IN1}, even if it is tied to RUN.

Since the output voltage of the charge pump can go above the input voltage, special circuitry is required to control the internal logic. Detection logic will draw an input current of 5µA when in shutdown. However, this current will be eliminated if the output voltage (V_{PUMP}) is less than approximately 0.8V.

The charge pump has built-in soft-start circuitry to prevent excessive current flow during start-up. The soft-start is achieved by charging an internal capacitor with a very weak current source. The voltage on this capacitor, in turn, slowly ramps the amount of current available to the output storage capacitor from zero to a value of 50mA over a period of approximately 125µs. The soft-start circuit is reset in the event of a commanded shutdown or thermal shutdown.

Light Load Current Operation (Burst Mode Operation, Pulse skipping or Continuous Conduction)

The LTC3852 can be enabled for high efficiency Burst Mode operation, constant frequency pulse skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select pulse skipping mode of operation, float the MODE/PLLIN pin or tie it to GND2. To select Burst Mode operation, tie MODE/PLLIN to $INTV_{CC}$ through a resistor no less than 50k, but no greater than 250k.

When the controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-fourth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.4V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom external MOSFET just before the

OPERATION

inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and constant frequency operation.

When the MODE/PLLIN pin is connected to GND2, the LTC3852 operates in PWM pulse skipping mode at light loads. At very light loads the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ/PLLFLTR and MODE/PLLIN Pins)

The selection of a switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3852's controller can be selected using the FREQ/PLLFLTR pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ/PLLFLTR pin can be used to program the controller's operating frequency from 250kHz to 750kHz.

A phase-locked loop (PLL) is available on the LTC3852 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller operates in forced continuous mode of operation when it is synchronized. A series RC should be connected between the FREQ/PLLFLTR pin and GND to serve as the PLL's loop filter.

It is suggested that the external clock be applied before enabling the controller unless a second resistor is connected in parallel with the series RC loop filter network. The second resistor prevents low switching frequency operation if the controller is enabled before the clock.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output of the step-down controller. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good (PGOOD) Pin

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±10% of the 0.8V reference voltage. The PGOOD pin is also pulled low when the RUN pin is low (shut down) or when the LTC3852's controller is in the soft-start or tracking phase. When the V_{FB} pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (abs max). The PGOOD pin will flag power good immediately when the V_{FB} pin is within the ±10% window. However, there is an internal 17µs power bad mask when V_{FB} goes out of the ±10% window.

Short-Circuit/Thermal Protection

The charge pump has built-in short-circuit current limit as well as over-temperature protection. During a short-circuit condition, it will automatically limit V_{PUMP} output current to approximately 300mA. At higher temperatures, or if the input voltage is high enough to cause excessive self-heating of the part, the thermal shutdown circuitry will shut down the charge pump once the junction temperature exceeds approximately 160°C. It will enable the charge pump once its junction temperature drops back to approximately 150°C. The charge pump will cycle in and out of thermal shutdown indefinitely until the short-circuit condition on V_{PUMP} is removed. The maximum rated junction temperature will be exceeded when this thermal shutdown protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a basic LTC3852 application circuit. The LTC3852 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice of the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 5.5V. Both SENSE pins are high impedance inputs with small base currents of less than 1µA. When the SENSE pins ramp up from 0V to 1.4V, the small base currents flow out of the SENSE pins. When the SENSE pins ramp down from 5V to 1.1V, the small base currents flow into the SENSE pins. The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2. R_{SENSE} is chosen based on the required output current. For simplicity, the charge pump section is omitted.

The current comparator has a maximum threshold, V_{MAX} = 50mV. The current comparator threshold sets the maximum peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. Allowing a margin of 20% for variations in the IC and external component values yields:

$$R_{SENSE} = 0.8 \bullet \frac{V_{MAX}}{I_{MAX} + \Delta I_L/2}$$

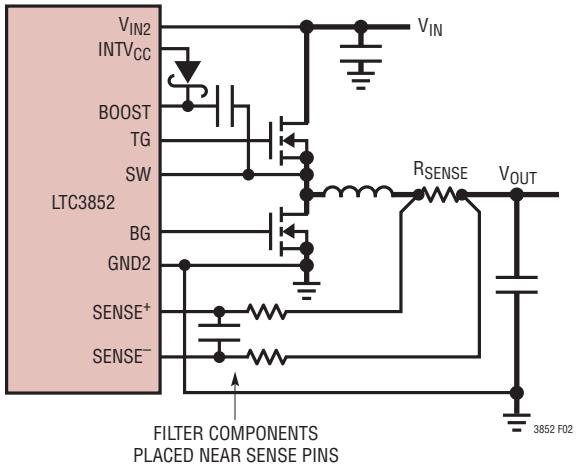


Figure 2. Using a Resistor to Sense Current with the LTC3852

Inductor DCR Sensing

For applications requiring the highest possible efficiency, the LTC3852 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by R2/(R1 + R2). Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. Check the manufacturer's data sheet for specifications regarding the inductor DCR, in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a good RLC meter.

APPLICATIONS INFORMATION

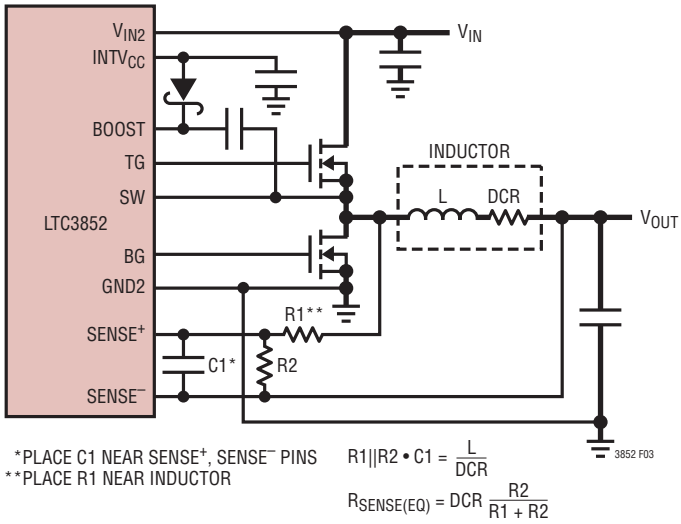


Figure 3. Current Mode Control Using the Inductor DCR

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC3852 uses a novel scheme that allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{f \bullet L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below ≈10% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for the LTC3852 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

APPLICATIONS INFORMATION

The peak-to-peak drive levels are set by the V_{PUMP} voltage. This voltage is typically 5V when the charge pump is active. Consequently, logic-level threshold MOSFETs may be used in most applications.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The optional Schottky diode conducts during the dead time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 2% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good size due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

Soft-Start and Tracking

The LTC3852 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When the LTC3852 is configured to soft-start by itself, a capacitor should be connected to the TRACK/SS pin. The LTC3852 is in the shutdown state if the RUN pin voltage is below 1.25V. TRACK/SS pin is actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.25V, the LTC3852 powers up. A soft-start current of 1µA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TRACK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is 0V to 0.8V on the TRACK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = 0.8 \bullet \frac{C_{SS}}{1.0\mu A}$$

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Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse skipping mode up to TRACK/SS = 0.64V. Between TRACK/SS = 0.64V and 0.72V, it will operate in forced continuous mode and revert to the selected mode once TRACK/SS > 0.72V. The output ripple is minimized during the 80mV forced continuous mode window.

When the regulator is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TRACK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, one can select the tracking resistive divider value to be small enough to make this error negligible.

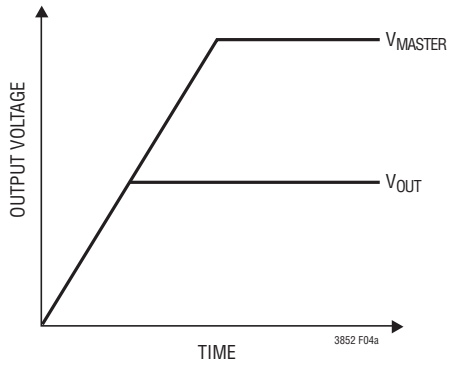
In order to track down another supply after the soft-start phase expires, the LTC3852 must be configured for forced continuous operation by connecting MODE/PLLIN to $INTV_{CC}$.

Output Voltage Tracking

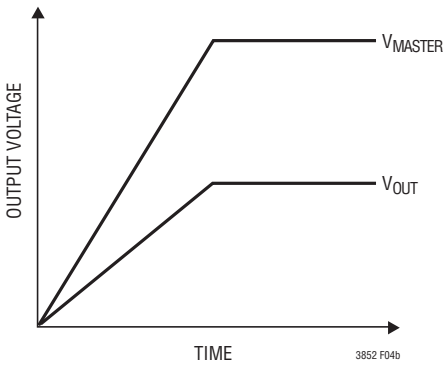
The LTC3852 allows the user to program how its output ramps up and down by means of the TRACK/SS pins. Through this pin, the output can be set up to either coincidentally or ratiometrically track with another supply's output, as shown in Figure 4. In the following discussions, V_{MASTER} refers to a master supply and V_{OUT} refers to the LTC3852's output as a slave supply. To implement the coincident tracking in Figure 4a, connect a resistor divider to V_{MASTER} and connect its midpoint to the TRACK/SS pin of the LTC3852. The ratio of this divider should be selected the same as that of the LTC3852's feedback divider as shown in Figure 5a. In this tracking mode, V_{MASTER} must be higher than V_{OUT}. To implement ratiometric tracking, the ratio of the resistor divider connected to V_{MASTER} is determined by:

$$\frac{V_{OUT}}{V_{MASTER}} = \frac{R2}{R4}\left(\frac{R3+R4}{R1+R2}\right)$$

So which mode should be programmed? While either mode in Figure 5 satisfies most practical applications, the coincident mode offers better output regulation. This concept can be better understood with the help of Figure 6. At the input stage of the LTC3852's error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TRACK/SS voltage is substantially higher than 0.8V at steady-state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB} and the internal precision 0.8V reference. In the ratiometric mode, however, TRACK/SS equals 0.8V at steady-state. D1 will divert part of the bias current to make V_{FB} slightly lower than 0.8V.



(4a) Coincident Tracking



(4b) Ratiometric Tracking

Figure 4. Two Different Modes of Output Voltage Tracking

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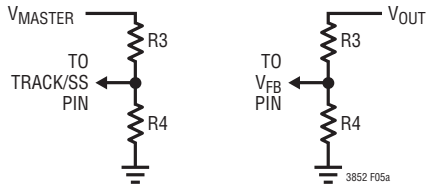
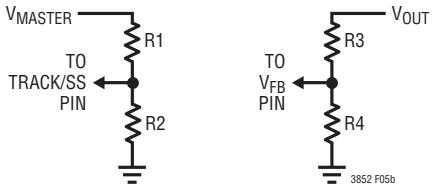


(5a) Coincident Tracking Setup



(5b) Ratiometric Tracking Setup

Figure 5. Setup for Coincident and Ratiometric Tracking

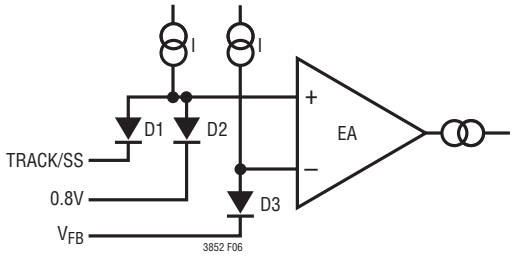


Figure 6. Equivalent Input Circuit of Error Amplifier

Although this error is minimized by the exponential I-V characteristic of the diode, it does impose a finite amount of output voltage deviation. Furthermore, when the master supply's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC}$$

The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET. The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

Undervoltage Lockout

The LTC3852 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out switching action when $INTV_{CC}$ falls below 3.25V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 400mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.25V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough.

C_{IN} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{O(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

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C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the effective series resistance, ESR, to minimize voltage ripple. The output ripple, ΔV_{OUT}, in continuous mode is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. With ΔI_L = $0.3I_{OUT(MAX)}$ and allowing 2/3 of the ripple to be due to ESR, the output ripple will be less than 50mV at maximum V_{IN} and:

$$C_{OUT} \text{ Required ESR} < 2.2R_{SENSE}$$

$$C_{OUT} > \frac{1}{8fR_{SENSE}}$$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

The selection of output capacitors for applications with large load current transients is primarily determined by the voltage tolerance specifications of the load. The resistive component of the capacitor, ESR, multiplied by the load current change, plus any output voltage ripple must be within the voltage tolerance of the load.

The required ESR due to a load current step is:

$$R_{ESR} \leq \frac{\Delta V}{\Delta I}$$

where ΔI is the change in current from full load to zero load (or minimum load) and ΔV is the allowed voltage deviation (not including any droop due to finite capacitance).

The amount of capacitance needed is determined by the maximum energy stored in the inductor. The capacitance must be sufficient to absorb the change in inductor current when a high current to low current transition occurs. The opposite load current transition is generally determined by the control loop OPTI-LOOP components, so make sure not to over compensate and slow down the response. The minimum capacitance to assure the inductors' energy is adequately absorbed is:

$$C_{OUT} > \frac{L(\Delta I)^2}{2(\Delta V)V_{OUT}}$$

where ΔI is the change in load current.

Manufacturers such as Nichicon, United Chemi-Con and Sanyo can be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductance effects.

In surface mount applications, ESR, RMS current handling and load step specifications may require multiple capacitors in parallel. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer surface mount capacitors offer very low ESR but have much lower capacitive density per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 1.5mm to 4.1mm. Aluminum electrolytic capacitors can be used in cost-driven applications, provided that consideration

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is given to ripple current ratings, temperature and long-term reliability. A typical application will require several to many aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, NEC Neocap, Panasonic SP and Sprague 595D series. Consult manufacturers for other specific recommendations.

Like all components, capacitors are not ideal. Each capacitor has its own benefits and limitations. Combinations of different capacitor types have proven to be a very cost effective solution. Remember also to include high frequency decoupling capacitors. They should be placed as close as possible to the power pins of the load. Any inductance present in the circuit board traces negates their usefulness.

Setting Output Voltage

The LTC3852 output voltage is set by an external feedback resistive divider carefully placed across the output, as shown in Figure 7. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1+\frac{R_B}{R_A}\right)$$

To improve the transient response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

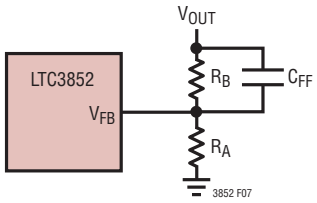

Figure 7. Settling Output Voltage

Fault Conditions: Current Limit and Current Foldback

The LTC3852 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 40% of its nominal output level, the maximum sense voltage is progressively lowered from its maximum programmed value to about 25% of the that value. Foldback current limiting is disabled during soft-start or tracking. Under short-circuit conditions with very low duty cycles, the LTC3852 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3852 (≈90ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is:

$$I_{SC} = \frac{1/4 Max V_{SENSE}}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Programming Switching Frequency

To set the switching frequency of the LTC3852, connect a resistor, R_{FREQ}, between FREQ/PLLFLTR and GND. The relationship between the oscillator frequency and R_{FREQ} is shown in Figure 8. A 0.1µF bypass capacitor should be connected in parallel with R_{FREQ}.

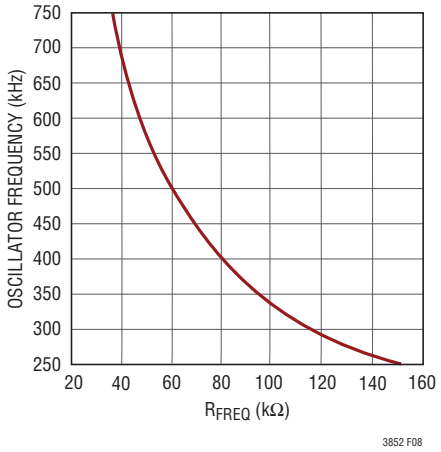

Figure 8. Relationship Between Oscillator Frequency and Resistor Connected Between FREQ/PLLFLTR and GND

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Phase-Locked Loop and Frequency Synchronization

The LTC3852 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (V_{CO}) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. This phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the FREQ/PLLFLTR pin. Note that the LTC3852 can only be synchronized to an external clock whose frequency is within range of the LTC3852's internal V_{CO}. This is guaranteed to be between 250kHz and 750kHz. A simplified block diagram is shown in Figure 9.

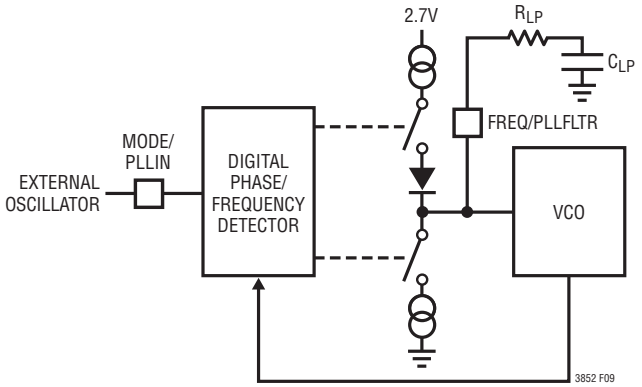

Figure 9. Phase-Locked Loop Block Diagram

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sunk continuously from the phase detector output, pulling down the FREQ/PLLFLTR pin. When the external clock frequency is less than f_{OSC}, current is sourced continuously, pulling up the FREQ/PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the FREQ/PLLFLTR pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} is 1k to 10k and C_{LP} is 2200pF to 0.01µF.

When the external oscillator is active before the LTC3852 is enabled, the internal oscillator frequency will track the external oscillator frequency as described in the preceding paragraphs. In situations where the LTC3852 is enabled before the external oscillator is active, a low free-running oscillator frequency of approximately 50kHz will result. It is possible to increase the free-running, pre-synchronization frequency by adding a second resistor in parallel with R_{LP} and C_{LP}. The second resistor will also cause a phase difference between the internal and external oscillator signals. The magnitude of the phase difference is inversely proportional to the value of the second resistor.

The external clock (on MODE/PLLIN pin) input high threshold is nominally 1.6V, while the input low threshold is nominally 1.2V.

Maximum Available Charge Pump Current

For the charge pump, the maximum available output current and voltage can be calculated from the effective open-loop output resistance, R_{OL}, and the effective input voltage, $2V_{IN1(MIN)}$.

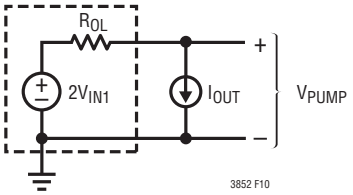

Figure 10. Equivalent Open-Loop Circuit

From Figure 10, the available current is given by:

$$I_{PUMP} = \frac{2V_{IN1} - V_{PUMP}}{R_{OL}}$$

The actual current (into V_{IN2} and $INTV_{CC}$) should not exceed 50mA.

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Effective Open Loop Output Resistance (R_{OL})

The effective open loop output resistance (R_{OL}) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator frequency (f_{OSC}), value of the flying capacitor (C_{FLY}), the nonoverlap time, the internal switch resistances (R_S), and the ESR of the external capacitors. A first order approximation for R_{OL} is given below:

$$R_{OL} \cong 2\sum_{S=1\ TO\ 4} R_S + \frac{1}{f_{OSC} \bullet C_{FLY}}$$

Typical R_{OL} values as a function of temperature are shown in Figure 11.

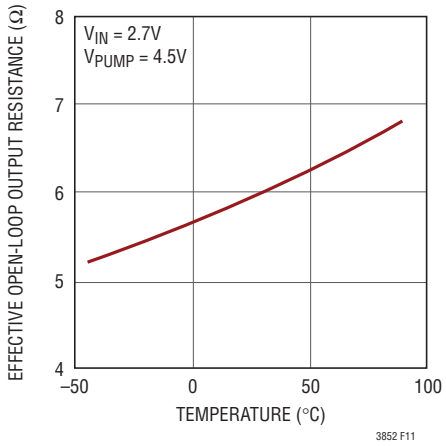

Figure 11. Typical R_{OL} vs Temperature

Charge Pump Capacitor Selection

The style and value of capacitors used with the charge pump determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low ESR (<0.1Ω) ceramic capacitors be used for both C_{IN} and C_{PUMP}. These capacitors should be 2.2µF or greater. Tantalum and aluminum capacitors are not recommended because of their high ESR.

The value of C_{PUMP} directly controls the amount of output ripple for a given load current. Increasing the size of C_{PUMP} will reduce the output ripple at the expense of higher minimum turn-on time. The peak-to-peak output ripple of a charge pump is approximately given by the expression:

$$V_{RIPPLE(P-P)} \cong \frac{I_{PUMP}}{2f_{OSC} \bullet C_{PUMP}}$$

where f_{OSC} is the charge pump frequency (typically 1.2MHz) and C_{PUMP} is the value of the V_{PUMP} storage capacitor.

Also, the value and style of the C_{PUMP} capacitor can significantly affect the stability of the charge pump. As shown in the Functional Diagram, the charge pump uses a linear control loop to adjust the strength of the charge pump to match the current required at the output. The error signal of this loop is stored directly on the output storage capacitor. This output capacitor also serves to form the dominant pole of the control loop. To prevent ringing or instability on the charge pump, it is important to maintain at least 1µF of capacitance over all conditions.

Excessive ESR on the C_{PUMP} capacitor can degrade the loop stability of the charge pump. Its closed loop output resistance is designed to be 0.5Ω. For a 50mA load current change, the output voltage will change by about 25mV. If the output capacitor has 0.5Ω or more of ESR, the closed loop frequency response will cease to roll off in a simple one-pole fashion and poor load transient response or instability could result. Ceramic capacitors typically have exceptional ESR performance and combined with a good board layout should yield very good stability and load transient performance.

As the value of C_{PUMP} controls the amount of output ripple, the value of C_{IN} controls the amount of ripple present at the input pin (V_{IN1}). The input current to the charge pump will be relatively constant during the input charging phase or the output charging phase but will drop to zero during the nonoverlap times. Since the nonoverlap time is small (~25ns), these missing notches will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the voltage drop in the ESR. Therefore, ceramic capacitors are again recommended for their exceptional ESR performance.

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Further input noise reduction can be achieved by powering V_{IN1} through a very small series inductor as shown in Figure 12. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

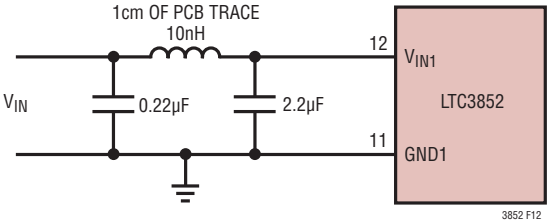

Figure 12. 10nH Inductor Used for Additional Input Noise Reduction

Flying Capacitor Selection

Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitor since its voltage can reverse upon start-up of the charge pump. Low ESR ceramic capacitors should always be used for the flying capacitor.

The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary to have at least 1µF of capacitance for the flying capacitor.

Ceramic Capacitors

Ceramic capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1µF 10V Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF 10V X7R capacitor available in the same 0603 case. In fact, for the charge pump, these capacitors can be considered roughly equivalent. The capacitor manufacturer's data sheet should be consulted to ensure the desired capacitance at all temperatures and voltages.

Table 1 shows a list of ceramic capacitor manufacturers and how to contact them:

Table 1.

AVX	www.avx.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
Vishay	www.vishay.com

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100. It is often useful to analyze the individual loss components to determine what limits the efficiency and which change would produce the biggest improvement. The efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, there are five main sources of power loss in LTC3851 circuits: 1) I^2R losses, 2) transition losses in the top MOSFET, 3) gate charge losses within the controller due to the input capacitance of the power MOSFETs, 4) the DC bias current of the controller (V_{IN2}), and 5) the efficiency of the charge pump.

1. I^2R losses are predicted from the DC resistances of the fuse (if used), top and bottom MOSFET on-resistances, the inductor DCR and the current sense resistor (if used). In continuous conduction mode (CCM), the average output current flows through the inductor (L) and sense resistor (R_{SENSE}), but is "chopped" between the top and bottom MOSFETs. Since the two MOSFETs rarely have the same R_{ON}, an effective MOSFET resistance

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can be computed using the duty cycle ($D = V_{OUT}/V_{IN}$). The effective MOSFET DC resistance is therefore:

$$R_{ON(EFF)} = D \bullet R_{ON(TOP)} + (1\text{-}D) \bullet R_{ON(BOT)}$$

The effective MOSFET resistance can then be summed with the DCR of the inductor and the sense resistor to obtain the overall series resistance. For example, consider a DC/DC converter with a 3.3V input voltage and a 1.2V/15A output. The nominal duty cycle of this converter is 36% (1.2V/3.3V). For a design with $R_{ON(TOP)}$ = 8mΩ and $R_{ON(BOT)}$ = 2mΩ, the effective MOSFET DC resistance is (0.36) • 0.008 + (1-0.36) • 0.002 = 4.2mΩ. For an inductor DCR = 1mΩ and a 2mΩ sense resistor, the total series resistance is 7.2mΩ. For an output current range of 5A to 15A, the total I^2R losses range from 1% to 9% for a 1.2V output. **It is worth noting that the losses due to the sense resistor at full load (15A) are 450mW, or 2.5%. If the same application used a DCR current sensing scheme, the peak efficiency would be 2.5% higher, an expensive component would be eliminated from the bill of materials, and the solution size would be smaller**. The efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

2. Since the LTC3852 was optimized for low supply voltage applications, the transition losses for the top MOSFET can normally be neglected. Transition losses for the top MOSFET only become significant when operating at high input voltages (typically 15V or greater). This condition can occur, however, when the input to the charge pump is not the same voltage as the input to the DC/DC converter power stage. For example, an auxiliary, low current 3.3V supply could be connected to the input of the charge pump (V_{IN1}), while the DC/DC converter power stage could draw power from a high current 12V supply. Transition losses for the upper power MOSFET can be estimated from the following equation:

$$\text{Transition Loss} = (1.7)V_{DS(MAX)}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f_{SW}$$

3. The $INTV_{CC}$ current is the sum of the MOSFET driver and DC bias requirements of the internal circuitry. The gate drive current results from charging the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched on, a packet of charge Q_G moves from $INTV_{CC}$ to the MOSFET gate. The resulting dQ/dt is a current into $INTV_{CC}$ that is typically much larger than the DC bias current for the internal control circuitry. In CCM operation, $I_{GATE} = f_{SW} \bullet (Q_{G(TOP)} + Q_{G(BOT)})$, where $Q_{G(TOP)}$ and $Q_{G(BOT)}$ are the gate charges of the top and bottom MOSFETs respectively. These parameters are listed on most power MOSFET datasheets.

4. The DC bias current for the controller is specified in the Electrical Characteristics table, and is typically 1.2mA. This current is almost always much smaller than the gate charge current associated with the power MOSFETs in CCM operation.

5. In most LTC3852 applications, the output of the charge pump will be connected to the V_{IN2} and $INTV_{CC}$ pins of the controller. The DC bias current into the controller V_{IN2} pin, as well as the gate charge current associated with the power MOSFETs, will typically be supplied by the charge pump. Because the charge pump has a finite power efficiency, the input current will be higher that the output current when the charge pump is active. For a 3.3V input application where the output of the charge pump is 5.1V, this efficiency is approximately 72%, as shown in the graph in the Typical Performance Characteristics. As a result, for every 1mA of current required by the controller, about 1.4mA will be drawn from the V_{IN1} pin.

The DC bias current of the charge pump within the LTC3852 is typically only 60µA. For the purposes of power losses, this bias current is typically 2 orders of magnitude lower than the gate drive current, and can therefore be neglected.

Other "hidden" losses such as copper trace and the battery internal resistance can account for an additional several percent efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require

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a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Typical Application circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The midband gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3852. These items are also illustrated graphically in the layout diagram of Figure 13. Check the following in your layout:

1. Are the board signal and power grounds segregated? The LTC3852 ground pins should connect to the ground plane close to the output capacitor(s). The low current or signal ground lines should make a single point tie directly to the GND1 and GND2 pins. The synchronous MOSFET source pins should connect to the input capacitor(s) ground.
2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal

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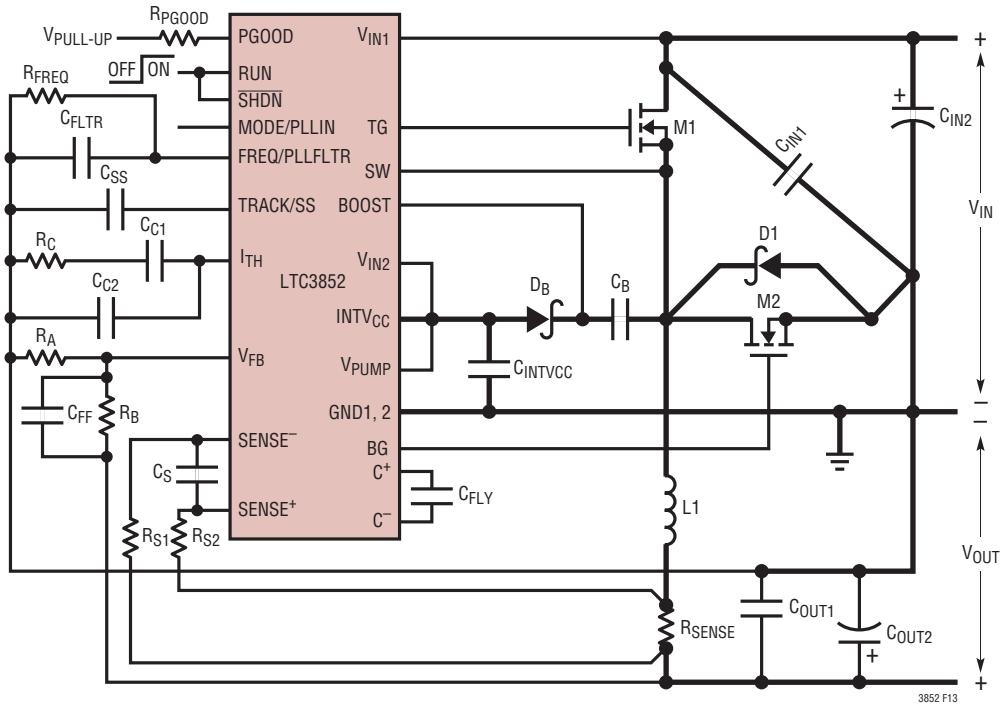

Figure 13. LTC3852 Switching Regulator Layout Diagram

ground. The 47pF to 100pF capacitor should be as close as possible to the LTC3852. Be careful locating the feedback resistors too far away from the LTC3852. The V_{FB} line should not be routed close to any other nodes with high slew rates.

3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE$^+$ and SENSE$^-$ should be as close as possible to the LTC3852. Ensure accurate current sensing with Kelvin connections as shown in Figure 14. Series resistance can be added to the SENSE lines to increase noise rejection and to compensate for the ESL of R_{SENSE}.

4. Does the (+) terminal of C_{IN} connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).

5. Is the $INTV_{CC}$ ceramic decoupling capacitor connected closely between $INTV_{CC}$ and GND2? This capacitor carries the MOSFET driver peak currents.

6. Keep the switching node (SW), top gate node (TG) and boost node (BOOST) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3852 and occupy minimum PC trace area.

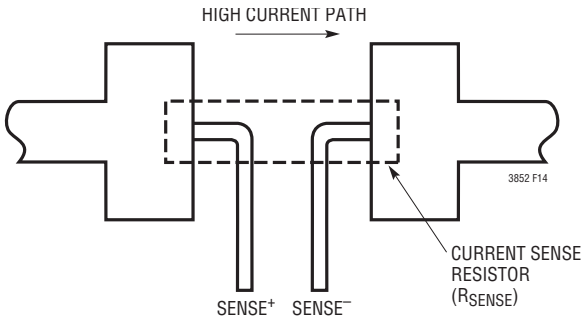

Figure 14. Kelvin Sensing R_{SENSE}

Layout Considerations (Charge Pump)

Due to the high switching frequency and high transient currents produced by the charge pump, careful board layout is necessary for optimum performance. A true ground plane and short connections to all the external capacitors

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will improve performance and ensure proper regulation under all conditions. Figure 15 shows an example layout for the charge pump.

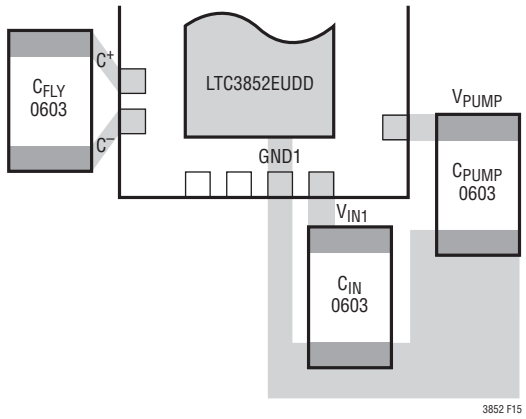

Figure 15. Recommended Charge Pump Layout

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pick-up at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the Schottky and the top MOSFET to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

Design Example

As a design example, assume V_{IN} = 3.3V (nominal), V_{IN} = 5.5V (maximum), V_{OUT} = 1.5V, I_{MAX} = 15A, and f = 400kHz (refer to Figure 16).

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Connect a 68.1k resistor between the FREQ/PLLFLTR and GND pins, generating 400kHz operation. The inductance for 30% ripple current is:

$$L = \frac{1}{\Delta I_L(f)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$= \frac{1}{4.5A(400kHz)} 1.5V\left(1-\frac{1.5V}{3.3V}\right) = 454nH$$

A 400nH inductor will produce 34% ripple current. The peak inductor current will be the maximum DC value (15A) plus one-half the ripple current (2.5A), or 17.5A. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{1.5V}{5.5V(400kHz)} = 682ns$$

which is greater than the 90ns minimum on-time.

The R_{SENSE} resistor value can be calculated by using the minimum current sense voltage specification with a 20% increase for current limit.

$$R_{SENSE} \le \frac{V_{SENSE(MIN)}}{I_{PEAK} \bullet 1.2} \le \frac{40mV}{17.5A \bullet 1.2} = 1.9m\Omega$$

Choosing 1% resistors: R1 = 20k and R2 = 37.4k yields an output voltage of 1.496V.

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The power dissipation on the topside MOSFET can be easily estimated. Choosing Vishay SIR438DP MOSFETs results in: $R_{DS(ON)}$ = 0.0023Ω, C_{MILLER} = 445pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{1.5V}{5.5V}(15)^2\left[1+(0.005)(50°C-25°C)\right]$$
$$\bullet(0.0023\Omega)+(5.5V)^2\left(\frac{15A}{2}\right)(2\Omega)(445pF)$$
$$\bullet\left[\frac{1}{5-1}+\frac{1}{1}\right](400kHz)=108mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC}=\frac{\left(\frac{1}{4}\right)65mV}{0.003\Omega}-\frac{1}{2}\left(\frac{90ns(5.5V)}{400nH}\right)=4.8A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC}=\frac{5.5V-1.5V}{5.5V}(15A)^2(1.125)(0.0023\Omega)=423mW$$

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 9A at temperature. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}\,(\Delta I_L) = 0.02\Omega\ (5.1A) = 102mV_{P-P}$$

TYPICAL APPLICATIONS

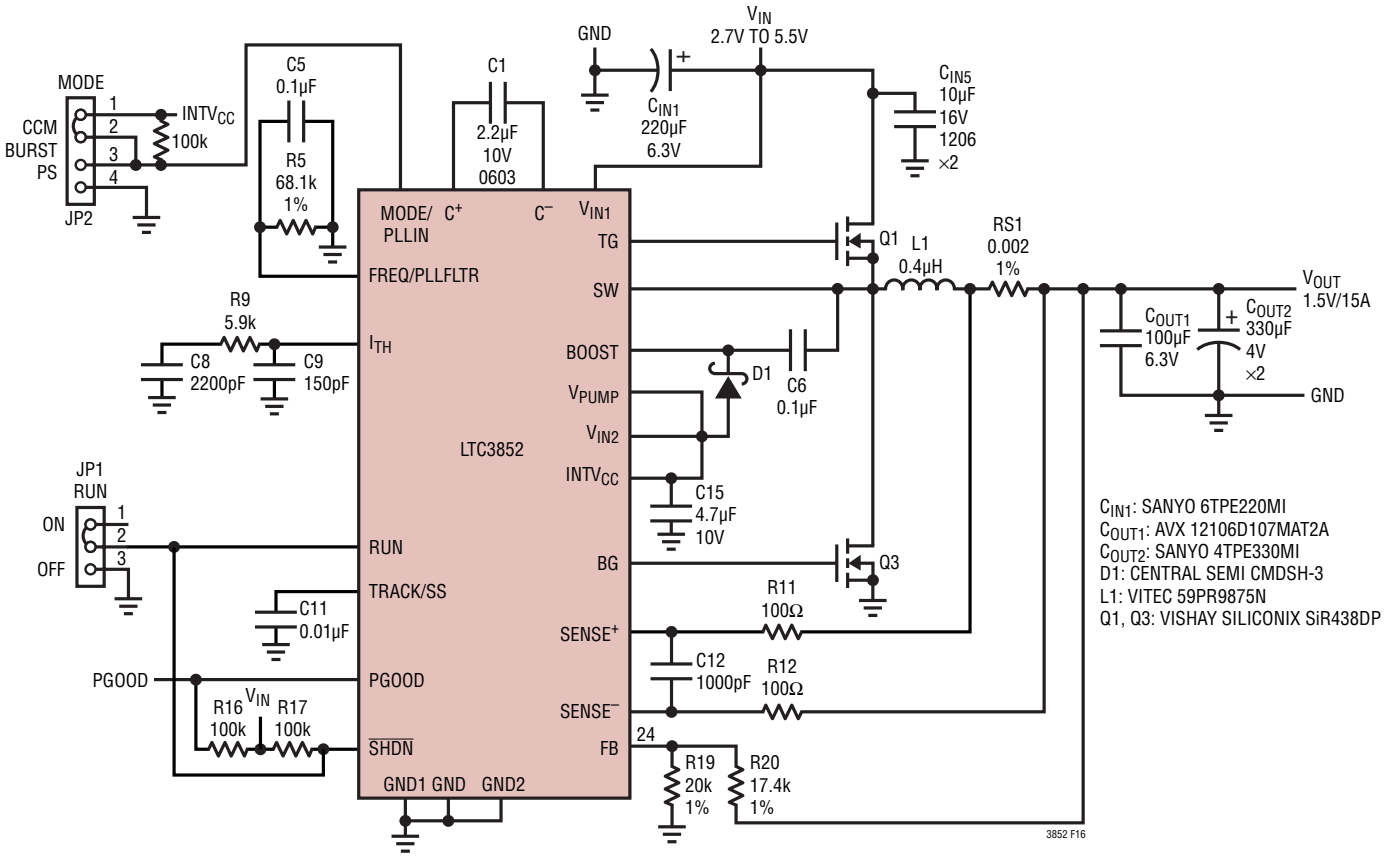


Figure 16. High Efficiency 1.5V/15A Step-Down Converter From Design Example

TYPICAL APPLICATIONS

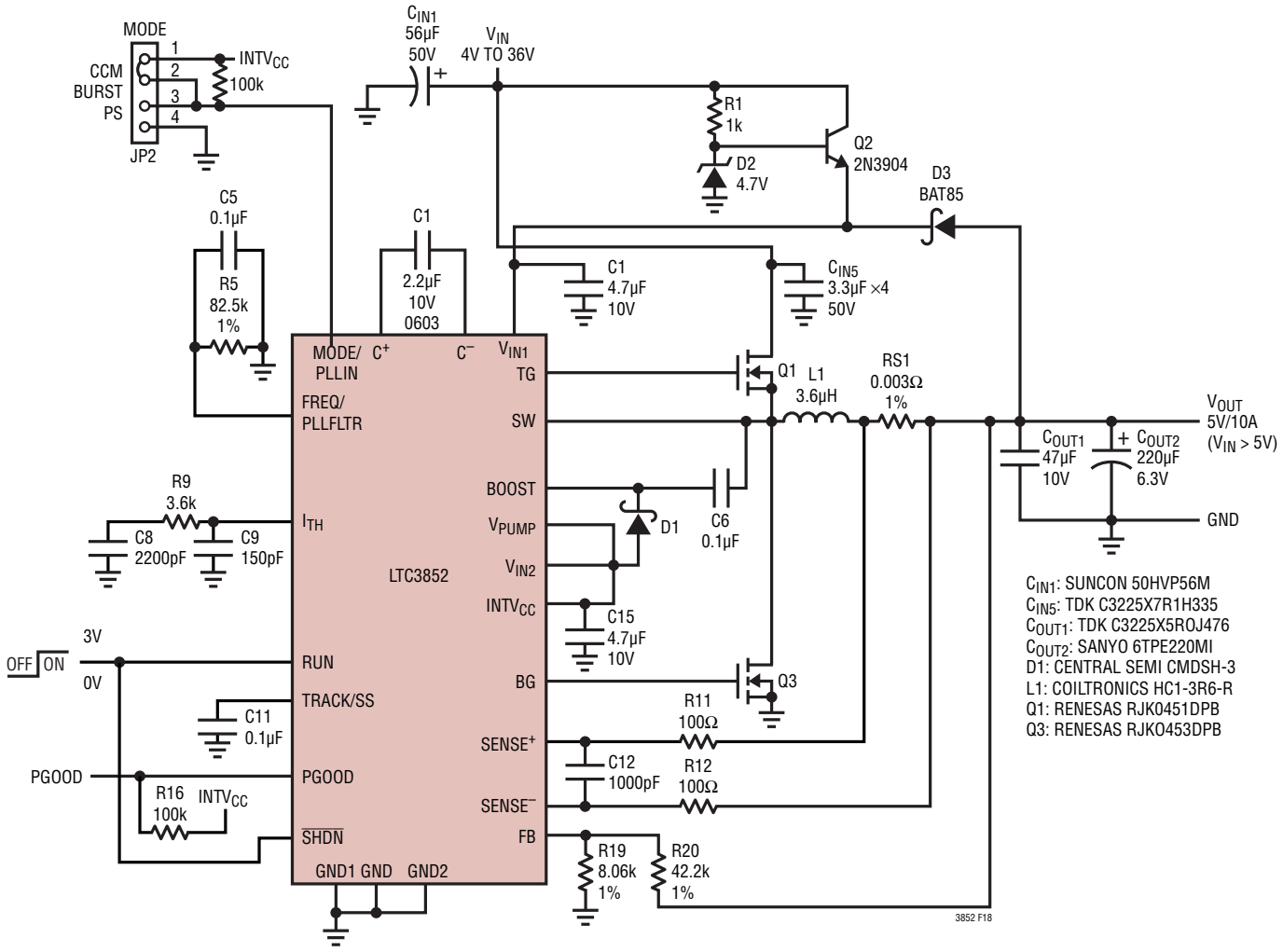
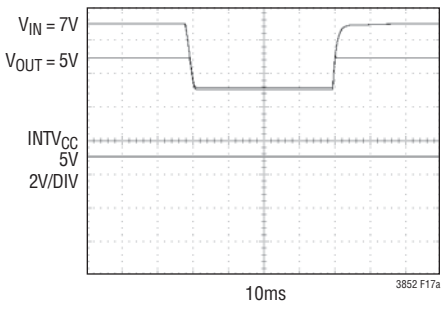


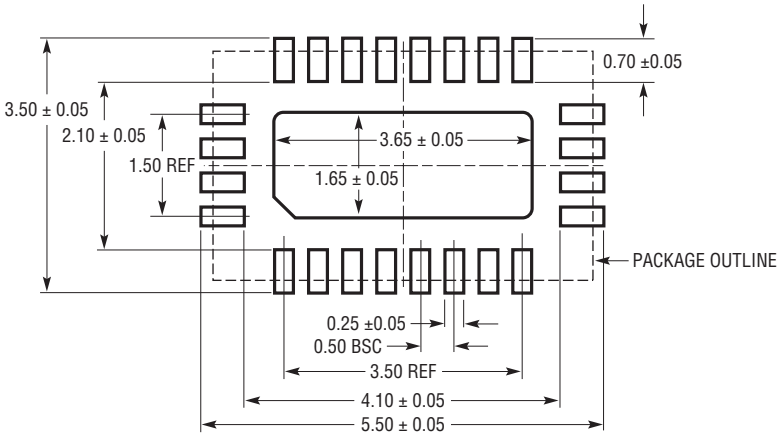
Figure 17. 5V/10A Converter Providing 5V Drive to MOSFETs for 4V < V_{IN} < 36V

$INTV_{CC}$ During Line Transient (V_{IN1} < 5V)

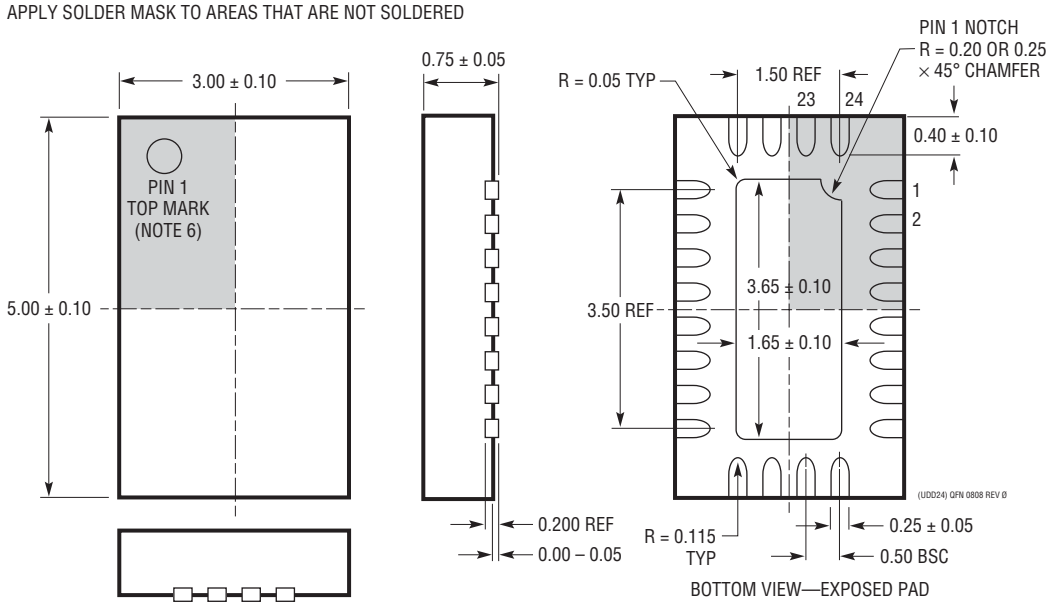


PACKAGE DESCRIPTION

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

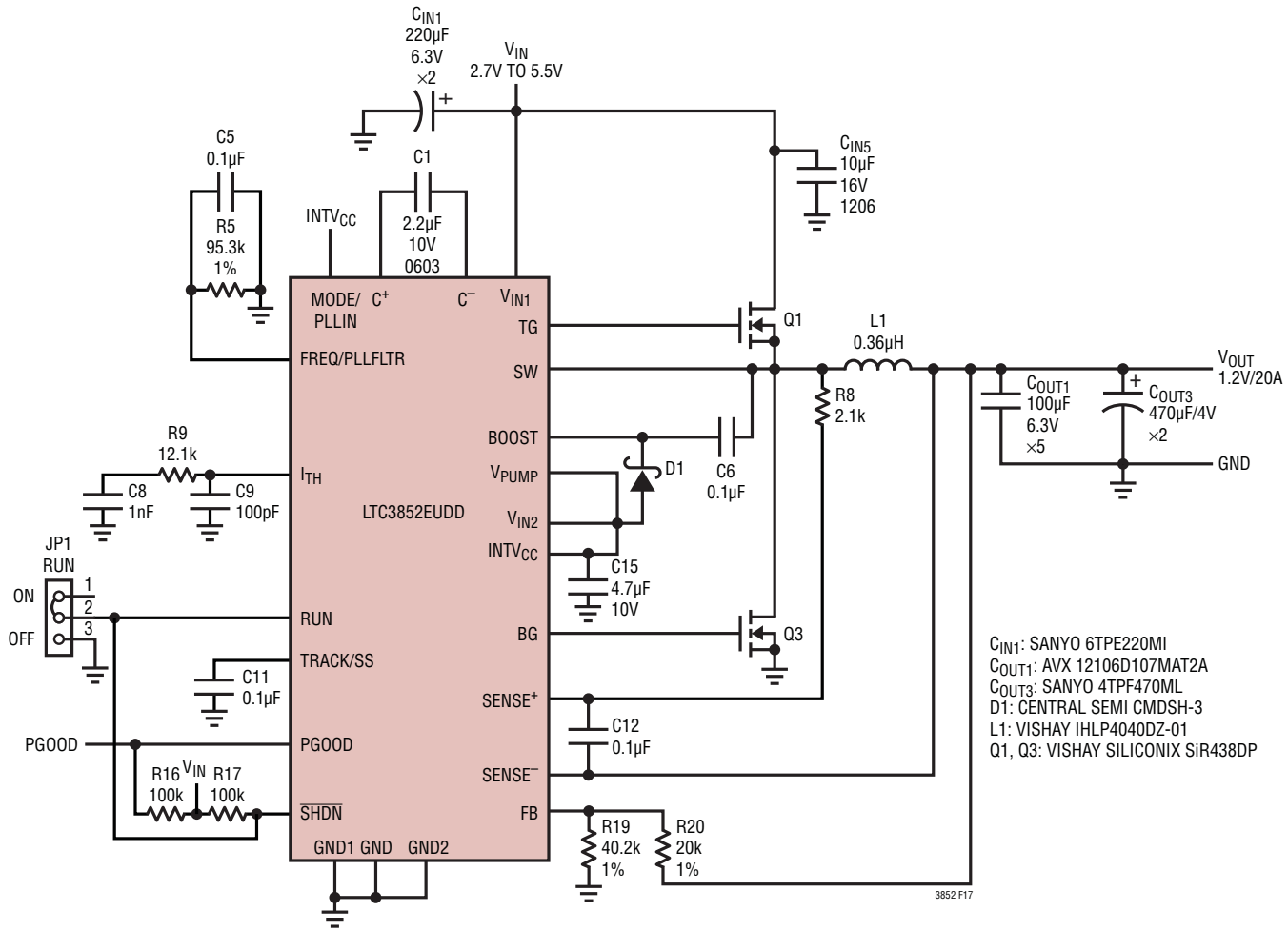


Figure 18. 1.2V/20A Low Ripple DCR Sense Application

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3736/LTC3736-1/ LTC3736-2	Dual, 2-Phase Synchronous Step-Down Controller	2.75V ≤ V_{IN} ≤ 9.8V, No R_{SENSE}™
LTC3772/LTC3772B	Micropower, No R_{SENSE} Constant Frequency Step-Down DC/DC Controller	2.75V ≤ V_{IN} ≤ 9.8V, No R_{SENSE}, 40µA No-Load I_Q
LTC3776	Dual 2-Phase, No R_{SENSE} Synchronous Controller for DDR/ QDR Memory Termination	2.75V ≤ V_{IN} ≤ 9.8V, V_{OUT2} Tracks 1/2 V_{REF}
LT3808	No R_{SENSE}, Low EMI, Synchronous DC/DC Controller with Output Tracking	2.75V ≤ V_{IN} ≤ 9.8V, Spread Spectrum Modulation for Low Noise
LTC3809/LTC3809-1	No RSENSE, Low Input Voltage, Synchronous DC/DC Controller	2.75V ≤ V_{IN} ≤ 9.8V, Output Tracking (LTC3809-1) or Spread Spectrum Modulation
LTC3822/LTC3822-1	Low Input Voltage Synchronous Step-Down Controller	2.75V ≤ V_{IN} ≤ 4.5V, No R_{SENSE}
LTC3836	Dual, Low Input Voltage Synchronous Step-Down Controller	2.75V ≤ V_{IN} ≤ 4.5V, No R_{SENSE}

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