BLF8G22LS-270V; Power LDMOS transistor Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

Product profile

1.1 General description

270 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 2110 MHz to 2170 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f	I _{Dq}	V _{DS}	$P_{L(AV)}$	Gp	η_{D}	ACPR _{5M}
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2110 to 2170	2400	28	80	17.3	29	-29 <u>[1]</u>

^{[1] 3}GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; 5 MHz carrier spacing.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation
- Decoupling leads to enable improved video bandwidth (80 MHz typical)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifiers for base stations and multi carrier applications in the 2110 MHz to 2170 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G22	2LS-270V (SOT1244B)		
1	drain	4 1 E	4
2	gate	4 1 5	6,7 → 1
3	source	[1]	2
4	video lead		3
5	video lead		aaa-003619
6	n.c.		
7	n.c.	6 2 7	
BLF8G22	2LS-270GV (SOT1244C)		
1	drain	4 1 5	1
2	gate	4 1 5	6,7 → 1 4,5
3	source	<u>[1]</u>	2
4	video lead		3
5	video lead	6 2 7	aaa-003619
6	n.c.	3	
7	n.c.		

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G22LS-270V	-	earless flanged ceramic package; 6 leads	SOT1244B
BLF8G22LS-270GV	-	earless flanged ceramic package; 6 leads S0	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 50 W	0.26	K/W

6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

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Parameter	Conditions	Min	Тур	Max	Unit
drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_{D} = 4.5 \text{ mA}$	65	-	-	V
gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 450 mA	1.5	1.8	2.3	V
drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	4.2	μΑ
drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	80	-	Α
gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	420	nΑ
forward transconductance	V_{DS} = 10 V; I_{D} = 450 mA	-	3.8	-	S
drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 15.75 \text{ A}$	-	0.04	-	Ω
	drain-source breakdown voltage gate-source threshold voltage drain leakage current drain cut-off current gate leakage current forward transconductance	$\begin{array}{ll} \mbox{drain-source breakdown voltage} & \mbox{$V_{\rm GS}$ = 0 V; I_D$ = 4.5 mA} \\ \mbox{gate-source threshold voltage} & \mbox{$V_{\rm DS}$ = 10 V; I_D$ = 450 mA} \\ \mbox{drain leakage current} & \mbox{$V_{\rm GS}$ = 0 V; $V_{\rm DS}$ = 28 V} \\ \mbox{drain cut-off current} & \mbox{$V_{\rm GS}$ = $V_{\rm GS(th)}$ + 3.75 V; } \\ \mbox{$V_{\rm DS}$ = 10 V$} \\ \mbox{gate leakage current} & \mbox{$V_{\rm GS}$ = 11 V; $V_{\rm DS}$ = 0 V$} \\ \mbox{forward transconductance} & \mbox{$V_{\rm DS}$ = 10 V; I_D$ = 450 mA} \\ \mbox{drain-source on-state resistance} & \mbox{$V_{\rm GS}$ = $V_{\rm GS(th)}$ + 3.75 V;} \\ \end{array}$	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$\begin{array}{llllllllllllllllllllllllllllllllllll$	$\begin{array}{llllllllllllllllllllllllllllllllllll$

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 2400 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	$P_{L(AV)} = 80 \text{ W}$	16.3	17.3	-	dB
RLin	input return loss	$P_{L(AV)} = 80 \text{ W}$	-	-17	-7	dB
η_{D}	drain efficiency	$P_{L(AV)} = 80 \text{ W}$	26	29	-	%
ACPR _{5M}	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 80 W$	-	-29	-26.5	dBc

7. Test information

7.1 Ruggedness in class-AB operation

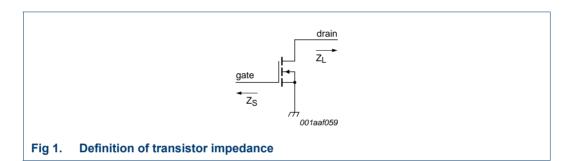
The BLF8G22LS-270V and BLF8G22LS-270GV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 2400 mA; P_L = 270 W (CW); f = 2110 MHz.

7.2 Impedance information

Table 8. Typical impedance information

 $I_{Dq} = 2400$ mA; main transistor $V_{DS} = 28$ V. Z_S and Z_L defined in Figure 1.

f	Z _S	Z _L
(MHz)	(Ω)	(Ω)
BLF8G22LS-270V		
2110	0.68 – j4.73	2.42 – j2.08
2140	0.80 – j4.94	2.67 – j2.24
2170	0.96 – j5.37	2.68 – j2.24
BLF8G22LS-270GV		
2110	1.23 – j6.94	2.39 – j4.22
2140	1.43 – j7.42	2.68 – j4.22
2170	1.44 – j7.50	2.90 – j4.30



7.3 Test circuit

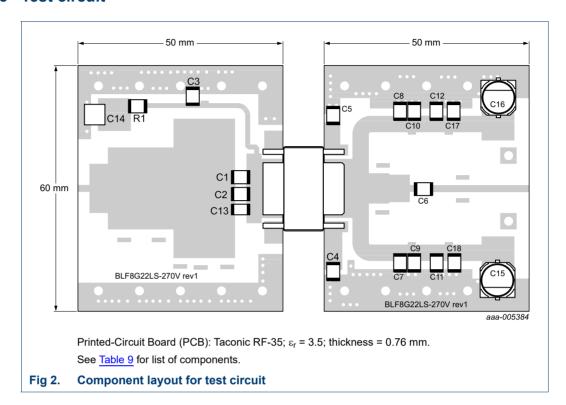
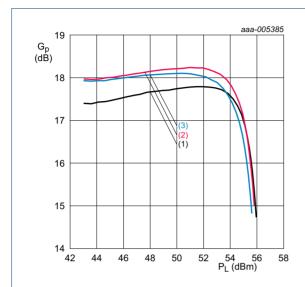


Table 9. List of components For test circuit, see Figure 2.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	0.7 pF	ATC100B
C3	multilayer ceramic chip capacitor	47 pF	ATC100B
C4, C5, C17, C18	multilayer ceramic chip capacitor	$4.7~\mu\text{F},50~\text{V}$	Murata
C6	multilayer ceramic chip capacitor	33 pF	ATC100B
C7, C8	multilayer ceramic chip capacitor	12 pF	ATC100B
C9, C10, C11, C12	multilayer ceramic chip capacitor	100 pF	ATC100B
C13	multilayer ceramic chip capacitor	0.2 pF	ATC100B
C14	multilayer ceramic chip capacitor	10 μ F, 50 V	Murata; SMD 2220
C15, C16	electrolytic capacitor	470 μ F, 63 V	
R1	resistor	5.1 Ω	SMD 1206; tolerance = 1 %

7.4 Graphs

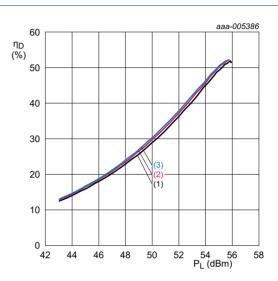
7.4.1 Pulsed CW



 V_{DS} = 28 V; I_{Dq} = 2400 mA; t_p = 100 $\mu s; \, \delta$ = 10 %.

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 3. Power gain as a function of output power; typical values

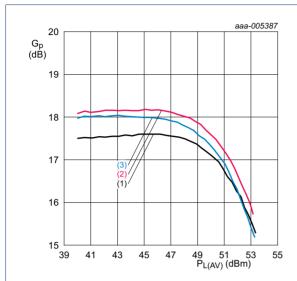


 V_{DS} = 28 V; I_{Dq} = 2400 mA; t_p = 100 μ s; δ = 10 %.

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 4. Drain efficiency as a function of output power; typical values

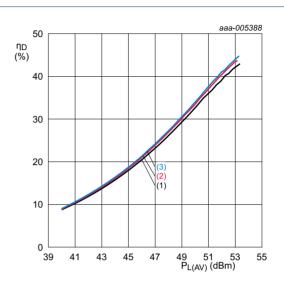
7.4.2 IS-95



 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

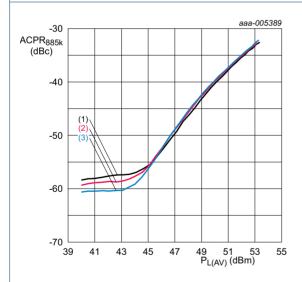
Fig 5. Power gain as a function of average output power; typical values



 V_{DS} = 28 V; I_{Dq} = 2400 mA.

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

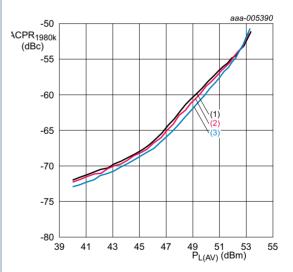
Fig 6. Drain efficiency as a function of average output power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Adjacent channel power ratio (885 kHz) as a Fig 7. function of average output power; typical values



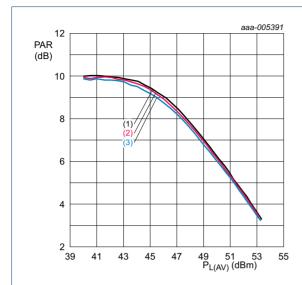
 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 8. Adjacent channel power ratio (1980 kHz) as a function of average output power; typical values

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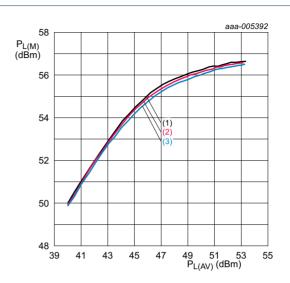
Power LDMOS transistor



 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 9. Peak-to-average power ratio as a function of average output power; typical values

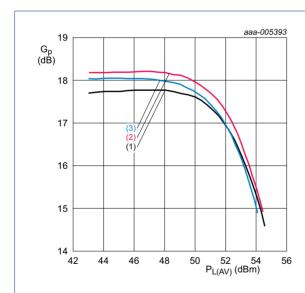


 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2110 MHz
- (2) f = 2140 MHz
- (3) f = 2170 MHz

Fig 10. Peak output power ratio as a function of average output power; typical values

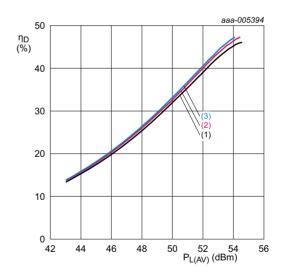
7.4.3 1-carrier W-CDMA



 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

Fig 11. Power gain as a function of average output power; typical values

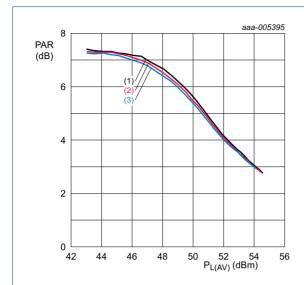


 V_{DS} = 28 V; I_{Dq} = 2400 mA.

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

Fig 12. Drain efficiency as a function of average output power; typical values

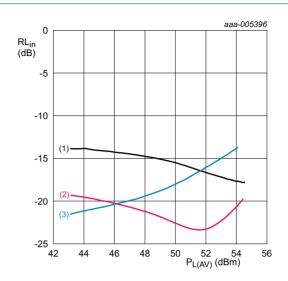
Power LDMOS transistor



 $V_{DS} = 28 \text{ V}; I_{Dq} = 2400 \text{ mA}.$

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

Fig 13. Peak-to-average power ratio as a function of average output power; typical values

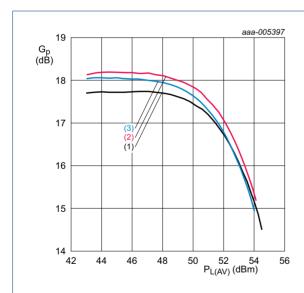


 V_{DS} = 28 V; I_{Dq} = 2400 mA.

- (1) f = 2112.5 MHz
- (2) f = 2140 MHz
- (3) f = 2167.5 MHz

Fig 14. Input return loss as a function of average output power; typical values

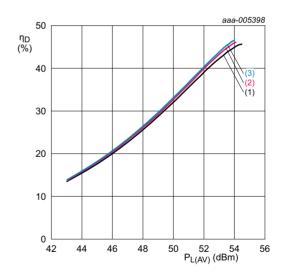
7.4.4 2-carrier W-CDMA



 V_{DS} = 28 V; I_{Dq} = 2400 mA; 5 MHz carrier spacing.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

Fig 15. Power gain as a function of average output power; typical values

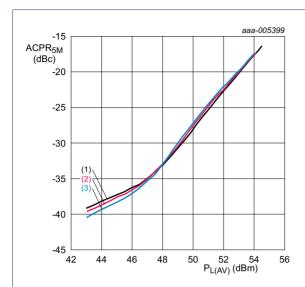


 V_{DS} = 28 V; I_{Dq} = 2400 mA; 5 MHz carrier spacing.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

Fig 16. Drain efficiency as a function of average output power; typical values

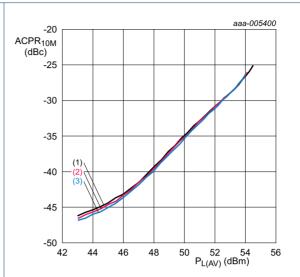
Power LDMOS transistor



 V_{DS} = 28 V; I_{Dq} = 2400 mA; 5 MHz carrier spacing.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

Fig 17. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values

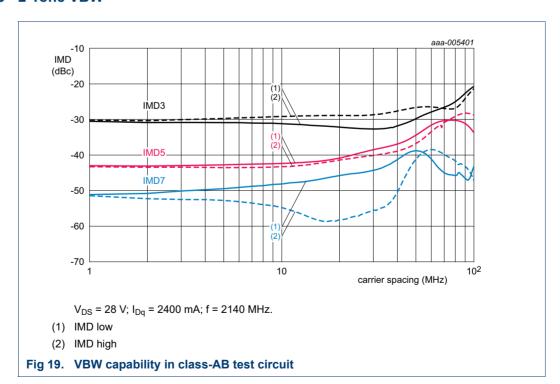


 V_{DS} = 28 V; I_{Dq} = 2400 mA; 5 MHz carrier spacing.

- (1) f = 2115 MHz
- (2) f = 2140 MHz
- (3) f = 2165 MHz

Fig 18. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

7.4.5 2-Tone VBW



8. Package outline

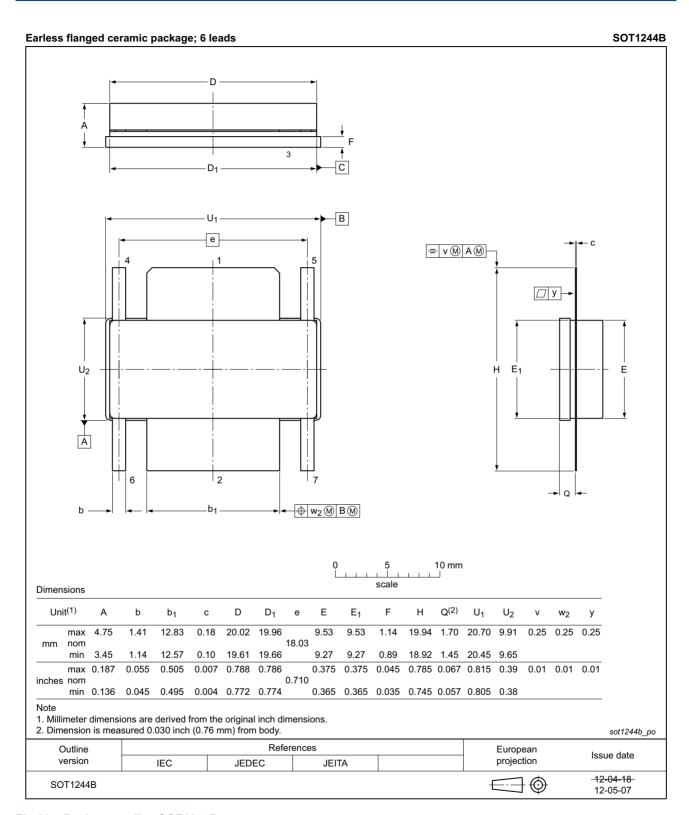


Fig 20. Package outline SOT1244B

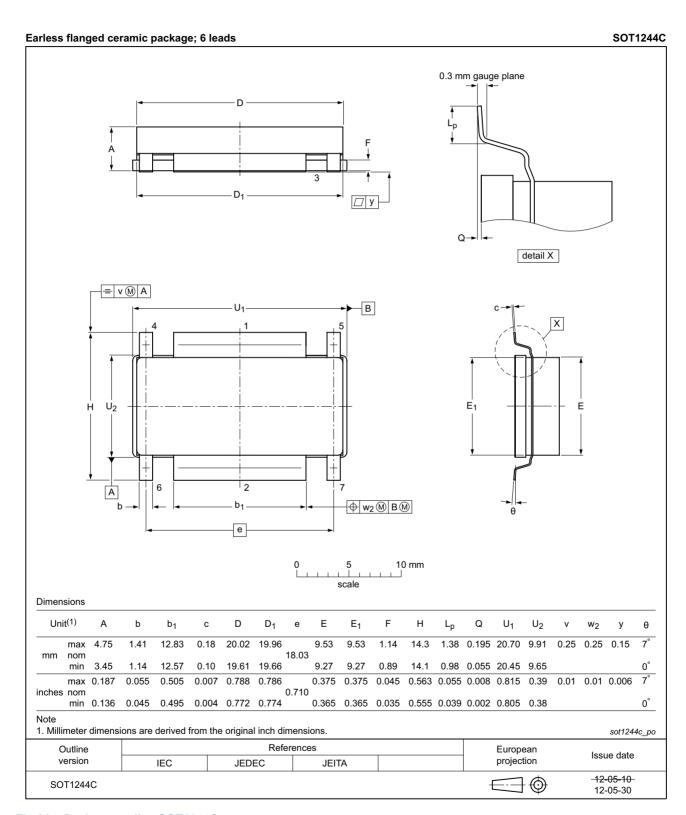


Fig 21. Package outline SOT1244C

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

A	Description
Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G22LS-270V_8G22LS-270GV#3	20150901	Product data sheet		BLF8G22LS-270V_8 G22LS-270GV v.2
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. 			
	 Legal texts have been adapted to the new company name where appropriate. 			
BLF8G22LS-270V_8G22LS-270GV v.2	20121203	Product data sheet	-	BLF8G22LS-270V_ 8G22LS-270GV v.1
BLF8G22LS-270V_8G22LS-270GV v.1	20120613	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition	
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.	
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.	
Product [short] data sheet	Production	This document contains the product specification.	

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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Power LDMOS transistor

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BLF8G22LS-270(G)V

Power LDMOS transistor

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.