

### STD840DN40

### Dual NPN high voltage transistors in a single package

Datasheet — production data

#### **Features**

- Low V<sub>CE(sat)</sub>
- Simplified circuit design
- Reduced component count
- Fast switching speed

### **Applications**

- Compact fluorescent lamp (CFL) 220 V mains
- Electronic ballast for fluorescent lighting



This device is a dual NPN high voltage power transistor manufactured using multi-epitaxial planar technology. It is housed in a dual-island DIP-8 package, with separated terminals for a high degree of mounting flexibility.

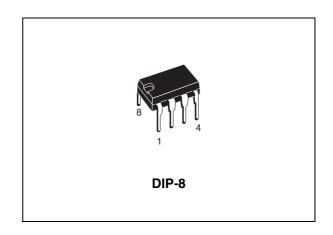


Figure 1. Internal schematic diagram

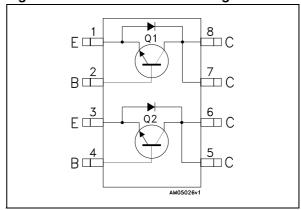


Table 1. Device summary

Order code	Marking	Package	Packaging
STD840DN40	D840DN40	DIP-8	Tube

Electrical ratings STD840DN40

# 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CBO</sub>	Collector-base voltage (I <sub>E</sub> = 0)	700	V
V <sub>CEO</sub>	Collector-emitter voltage (I <sub>B</sub> = 0)	400	٧
V <sub>EBO</sub>	Emitter-base voltage ( $I_C = 0$ , $I_B = 1.5$ A, $t_p < 10$ ms)	V <sub>(BR)EBO</sub>	٧
I <sub>C</sub>	Collector current	4	Α
I <sub>CM</sub>	Collector peak current (t <sub>P</sub> < 5 ms)	8	Α
I <sub>B</sub>	Base current	1.5	Α
I <sub>BM</sub>	Base peak current (t <sub>P</sub> < 5 ms)	3	Α
В.	Total dissipation at T <sub>amb</sub> = 25 °C single transistor	3	W
P <sub>TOT</sub>	Total dissipation at T <sub>case</sub> = 25 °C single transistor	45	W
T <sub>STG</sub>	Storage temperature	-65 to 150	°C
T <sub>J</sub>	Max. operating junction temperature	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thJA</sub> <sup>(1)</sup>	Thermal resistance junction-ambient (single transistor)	42	°C/W
R <sub>thJC</sub>	Thermal resistance junction-case (single transistor)	2.7	°C/W

<sup>1.</sup> Device mounted on PCB area of 25 mm<sup>2</sup>.

### 2 Electrical characteristics

 $T_{case}$  = 25 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Тур.	Max.	Unit
I <sub>CES</sub>	Collector cut-off current (V <sub>BE</sub> = 0)	V <sub>CE</sub> = 700 V V <sub>CE</sub> = 700 V T <sub>c</sub> =	125 °C			100 500	μ <b>Α</b> μ <b>Α</b>
I <sub>CEO</sub>	Collector cut-off current (I <sub>B</sub> = 0)	V <sub>CE</sub> = 400 V				250	μΑ
V <sub>(BR)EBO</sub>	Emitter-base breakdown voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = 10 mA		9		18	٧
V <sub>CEO(sus)</sub> <sup>(1)</sup>	Collector-emitter sustaining voltage (I <sub>B</sub> = 0)	I <sub>C</sub> = 10 mA		400			V
V <sub>CE(sat)</sub> <sup>(1)</sup>	Collector-emitter saturation voltage		$I_B = 0.2 A$ $I_B = 0.4 A$			0.5 1	V V
V <sub>BE(sat)</sub> <sup>(1)</sup>	Base-emitter saturation voltage		$I_B = 0.2 A$ $I_B = 0.4 A$			1.2 1.3	V V
h <sub>FE</sub> <sup>(1)</sup>	DC current gain	•	V <sub>CE</sub> = 5 V V <sub>CE</sub> = 5 V	10 8		24	
V <sub>F</sub>	Diode forward voltage	I <sub>F</sub> = 1 A				2.5	٧
t <sub>s</sub>	Resistive load Storage time Fall time	$I_{C} = 1 \text{ A}$ $I_{B1} =  V_{CC} = 125 \text{ V}$ $t_{i}$			2.5 0.2		μs μs

<sup>1.</sup> Pulse test: pulse duration ≤300 µs, duty cycle ≤ 2 %.

#### 2.1 Electrical characteristics (curves)

Figure 2. DC current gain  $(V_{CE} = 1 V)$ 

Figure 3. DC current gain  $(V_{CE} = 5 V)$ 

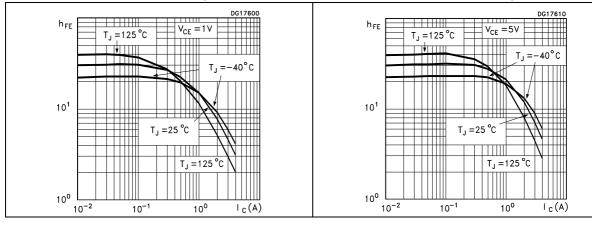


Figure 4. Collector-emitter saturation voltage Figure 5. Base-emitter saturation voltage

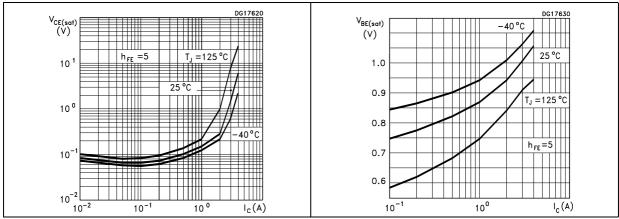
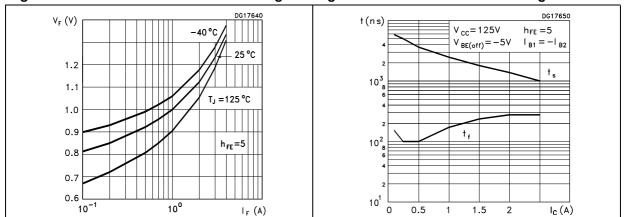


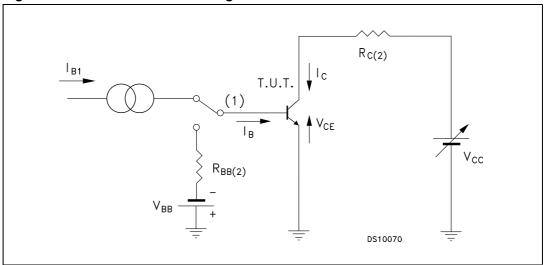
Figure 6. Freewheel diode forward voltage Figure 7. Resistive load switching time



STD840DN40 Test circuit

## 3 Test circuit

Figure 8. Resistive load switching test circuit



- 1. Fast electronic switch
- 2. Non-inductive resistor

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK<sup>®</sup> is an ST trademark.

Table 5. DIP-8 mechanical data

Dim.		mm.	
	Min.	Тур.	Max.
А			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
С	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
е		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

GC GAUGE PLANE 0.38 eЯ eВ  $\Box$ エ E1 A 1 A3 8145726\_A

Figure 9. Drawing dimension DIP-8

Revision history STD840DN40

# 5 Revision history

Table 6. Document revision history

Date	Revision	Changes
18-Nov-2009	1	Initial release.
16-Apr-2010	2	Inserted P <sub>TOT</sub> and R <sub>thJA</sub> values <i>Table 2</i> and <i>Table 3 on page 2</i> .
23-Oct-2012	3	Modified P <sub>TOT</sub> and R <sub>thJA</sub> values in <i>Table 2</i> and <i>Table 3 on page 2</i> . Minor text changes.

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