19-0703; Rev 1; 5/08

MAX19692/MAX19693 Evaluation Kits

Evaluate: MAX19692/MAX19693

General Description

The MAX19692/MAX19693 evaluation kits (EV kits) are fully assembled and tested PCBs that contain all the components necessary to evaluate the performance of the MAX19692 2.3Gsps and MAX19693 4.0Gsps 12-bit, direct RF synthesis digital-to-analog converters (DACs). The EV kit boards include wideband transformers for differential-to-single-ended conversion of the DAC output and for single-ended-to-differential conversion of the DAC clock.

Ordering Information

PART	TYPE
MAX19692EVKIT	EV Kit
MAX19693EVKIT	EV Kit
LVDSADPB12+	Adapter Board

+Denotes lead-free and RoHS compliant.

Features

- **2.3Gsps Maximum DAC Update Rate (MAX19692)**
- **4.0Gsps Maximum DAC Update Rate (MAX19693)**
- **Direct Interface with Maxim HSDCEP Data Source Board Using QSH Connectors**
- **Proven 12-Layer PCB Design**
- **On-Board Reference Circuitry**
- **On-Board Power-On Reset**
- **On-Board Clock Interface**
  2.3GHz Maximum Clock Rate (MAX19692)
  2.0GHz Maximum Clock Rate (MAX19693)
- **Wideband Output Transformer**
  Supports from < 30MHz to > 2000MHz
- **Fully Assembled and Tested**
- **Data Source (FPGA) Board Available (Order HSDCEP)**

Component Lists

MAX19692/MAX19693 EV Kits

DESIGNATION	QTY	DESCRIPTION
CLK, OUT	2	0.92in SMA connectors (PC edge mount)
C1, C2	2	100pF ±5%, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H101J or Murata GRM1555C1H101J
C3, C4, C12, C13	4	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M
C5–C8, C24–C31	12	1µF ±20%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J105M
C9, C10, C11	0	Not installed, ceramic capacitors (0603)
C14, C15, C16	3	47µF ±20% 16V tantalum capacitors (C case) AVX TPSC476M016R0350 or Vishay 594D476X0016C2T
C17–C23	7	10µF ±20%, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J106M or Murata GRM21BR60J106M
C32–C47	16	0.1µF ±20% 6.3V X5R ceramic capacitors (0201) TDK C0603X5R0J104M
DATA-CLKN, DATA-CLKP	0	Not installed, SMA PC-mount connectors (vertical)

DESIGNATION	QTY	DESCRIPTION
H1, H2	2	Vertical 2 x 60 surface-mount high-speed socket connectors Samtec QSH-060-01-L-D-A
JU1, JU2, JU7, JU8	4	2-pin headers
JU3, JU4, JU5, JU9*	4	3-pin headers
JU6	0	Not installed, 2-pin header
L1, L2, L3	3	Chip bead cores (1812) Panasonic EXC-CL4532U1
L4, L5	2	2.2µH wire-wound chip inductors (2520) Coilcraft 1008CS-222XJLB
R1	1	10kΩ ±5% resistors (0402)
R2, R3	0	Not installed, resistors (0402)
R4	0	Not installed, resistor (0603)
R5, R6	2	49.9Ω ±1% resistors (0402)
R7	1	2.0kΩ ±0.1% resistor (0402)
R8	1	499Ω ±1% resistor (0402)
R9, R11	2	174kΩ ±1% resistors (0603)
R10, R12	2	100kΩ ±1% resistors (0603)
SW1	1	Momentary pushbutton switch
T1–T4	4	1:1 3000MHz RF transformers Mini-Circuits TC1-1-13M+
TP1	0	Not Installed, PC test point

Component Lists (continued)

DESIGNATION	QTY	DESCRIPTION
U1	1	See the *EV Kit-Specific Component List*
U2	1	High-accuracy supervisory circuit (6 SOT23) Maxim MAX6710LUT+ (Top Mark: AAZL)
U3	1	1.25V precision voltage reference (8 SO) Maxim MAX6161AESA+ or Maxim MAX6161BESA+
—	8	Shunts (JU1–JU5, JU7, JU8, JU9*)
—	1	PCB: MAX19692/MAX19693 Evaluation Kit

**Not installed on the MAX19693 EV kit.*

EV Kit-Specific Component List

EV KIT PART NUMBER	DESIGNATION	DESCRIPTION
MAX19692EVKIT	U1	12-bit, 2.3Gsps, D-to-A converter (169 CSBGA) Maxim MAX19692EXW-D
MAX19693EVKIT		12-bit, 4.0Gsps, D-to-A converter (169 CSBGA) Maxim MAX19693EXW-D

Quick Start

Required Equipment

Before beginning, the following equipment is needed:

- Two 1.8V, 1A DC power supplies
- One 3.3V, 1A DC power supply
- Signal generator with low phase noise and low jitter for clock input signal (e.g., Agilent 8665B)
- One high-performance spectrum analyzer (e.g., Rohde & Schwarz FSU or Agilent PSA)
- One Maxim HSDCEP data source board
- (Optional) One Maxim LVDS adapter board when using a pattern generator with 0.1in header connectors (order the LVDSADPB12+ adapter board from Maxim Integrated Products, Inc.)

Procedure

The EV kits are fully assembled and tested. Follow the steps below to verify board operation. **Caution: Do not turn on the power supplies or signal sources until all connections are completed.**

LVDSADPB12 Adapter Board

DESIGNATION	QTY	DESCRIPTION
H1A, H2A	2	Vertical 2 x 60 surface-mount high-speed socket connectors Samtec QTH-060-01-F-D-A
J1–J4	4	Dual-row, 48-pin (2 x 24) headers
—	1	PCB: 12-Bit LVDS Adapter Board+

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corporation	843-946-0238	www.avxcorp.com
Coilcraft, Inc.	847-639-6400	www.coilcraft.com
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
Panasonic Corp.	800-344-2112	www.panasonic.com
TDK Corp.	847-803-6100	www.component.tdk.com
Vishay	402-563-6866	www.vishay.com

Note: *Indicate that you are using the MAX19692 or MAX19693 when contacting these component suppliers.*

1) Verify that shunts are installed in the following positions:

   JU1, JU2 (installed) → On-board reference enabled
   JU3 (2-3) → No delay added
   JU4 (2-3) → Modulation disabled (MAX19693 EV kit)
   JU4, JU9 (2-3) → Normal DAC (NRZ) operation (MAX19692 EV kit)
   JU5 (1-2) → DDR mode
   JU7 (installed) → Scan disabled (MAX19693 EV kit)/connect pin to ground (GND) (MAX19692 EV kit)
   JU8 (installed) → Calibration circuit enabled

2) Connect a 1.8V DC power supply to the VDD1.8 and GND pads.
3) Connect a 1.8V DC power supply to the AVCLK and GND pads.
4) Connect a 3.3V DC power supply to the AVDD3.3 and GND pads.
5) Connect the clock signal generator to the EV kit SMA connector labeled CLK.
6) Connect the Maxim HSDCEP data source board to connectors H1 and H2 on the EV kit. Download the latest version of the MAX19692 or MAX19693 EV kit firmware to the HSDCEP data source board

from www.maxim-ic.com/HSDCEP_Firmware and refer to the HSDCEP data sheet for upload and installation instructions. See the *Using the HSDCEP Data Source Board with the EV Kit* section.

7) Connect the spectrum analyzer to the EV kit SMA connector labeled OUT.
8) Turn on all the DC power supplies.
9) Enable the HSDCEP data source board.
10) Observe the output spectrum on the spectrum analyzer.

_Detailed Description of Hardware

The MAX19692 and MAX19693 EV kits are designed to simplify the evaluation of the MAX19692 2.3Gsps and MAX19693 4.0Gsps 12-bit, direct RF synthesis DACs. Each EV kit operates with LVDS data inputs, a single-ended clock input signal, and 1.8V/3.3V power supplies for simple board operation.

The EV kit PCB features on-board QSH connectors that interface directly to the Maxim HSDCEP data source board, circuitry that converts the differential 50Ω output to a single-ended 50Ω signal, and circuitry to convert a user-supplied single-ended clock signal to a differential clock required by the DAC. The EV kit also includes jumpers that configure frequency response, modulation, scan, reference voltage, calibration, and data clock modes.

Power Supplies

Each EV kit operates from two 1.8V and one 3.3V power supplies. The two separate 1.8V power supplies can be driven from the same source. Each power plane on the EV kit PCB is filtered for optimum dynamic performance.

Clock Signal

Each DAC requires a differential clock input signal with minimal jitter. The EV kits feature single-ended-to-differential-conversion circuitry. Supply a single-ended clock signal at the SMA connector labeled CLK. The power applied to the SMA should be between +10dBm and +15dBm when measured at the connector. Insertion losses due to the interconnecting cable decrease the power seen at the EV kit input. Account for these losses when setting the signal generator amplitude.

Reference Voltage Options

The DAC requires a reference voltage to set its output power. The DAC features a stable on-chip bandgap reference of 1.2V. The internal reference can be overdriven by an external reference to enhance accuracy and drift performance or for gain control.

The EV kit circuit features three reference options. Use the DAC's internal voltage reference by removing the shunts from jumpers JU1 and JU2. Use an external reference by removing the shunts from jumpers JU1 and JU2 and connecting a stable voltage reference at the REFIO pad. Install shunts on jumpers JU1 and JU2 to use the EV kit's on-board reference (MAX6161). See Table 1 to configure the shunts across jumpers JU1 and JU2 and select the source of the reference voltage.

Table 1. Reference Voltage Selection (JU1, JU2)

SHUNT POSITIONS	VOLTAGE REFERENCE MODE
Installed*	External 1.25V reference (U3) connected to DAC's REFIO pin
Not Installed	DAC's internal 1.2V bandgap reference
	User-supplied voltage reference at the REFIO pad (0.5V to 1.8V)

**Default position: JU1 (installed), JU2 (installed).*

The full-scale output power is dependent on the value of the reference voltage and the value of resistor R7. Use the equation below to calculate the DAC full-scale output power:

$$P_{OUT} = 20 \times \log\left[\frac{\left(32 \times \frac{V_{REFIO}}{R7} \times 23.5\right)}{0.6328}\right] [dBm]$$

where:

P_{OUT} = DAC full-scale output power

V_{REFIO} = voltage present at the REFIO pad (V_{REFIO} = 1.2V when using the DAC's internal reference)

R7 = value of resistor R7 in ohms (2kΩ default)

Data Clock Division

The data clock output differential signal (DATACLK) frequency is scaled down from the DAC clock input. Jumper JU5 controls the division factor. See Table 2 for shunt settings. Refer to the IC data sheet for details on synchronizing the DAC to an external pattern generator. Install resistors R2, R3, and R4 to access the differential output data clock signal at the DATA-CLKP and DATA-CLKN SMA connectors on the EV kit board when not using the Maxim HSDCEP data source board.

Table 2. Data Clock Division (JU5)

SHUNT POSITION	CLKDIV PIN	EV KIT FUNCTION
1-2	Connected to AVDD3.3	DDR mode: DATACLK = input data rate/2
2-3*	Connected to GND	QDR mode: DATACLK = input data rate/4

**Default position.*

Data Clock Delay

Jumper JU3 adjusts the delay of the data clock output. Refer to the *Data Timing Relationships* section in the IC data sheet for more details. See Table 3 for shunt settings.

Table 3. Data Clock Delay (JU3)

SHUNT POSITION	DELAY PIN	EV KIT FUNCTION
1-2	Connected to AVDD3.3	Delay of 1/2 input data period
2-3*	Connected to GND	No delay added

**Default position.*

Differential Output

The DAC features a differential output with built-in self-calibrated output termination resistors. The EV kit pulls the outputs up to AVDD3.3 through on-board bias inductors L4 and L5 to optimize performance of the device. Balun transformer T1 converts the differential signal to a single-ended signal. Measure the resulting DAC output at the SMA connector labeled OUT.

Impulse/Frequency Response (MAX19692)

The MAX19692 DAC has three impulse/frequency response modes: NRZ, RZ, and RF. These modes are set with the RZ and RF input pins. The MAX19692 EV kit provides jumpers JU4 and JU9 to configure these pins. See Table 4 for jumpers JU4 and JU9 configuration. Refer to the *DAC Impulse/Frequency Response Modes* section in the MAX19692 IC data sheet for more details.

Table 4. RZ and RF Input Configuration (JU4, JU9)

SHUNT POSITION		FREQUENCY RESPONSE MODE
JU4	JU9	
2-3*	2-3*	NRZ
2-3	1-2	RZ
1-2	2-3	RF

**Default position.*

Modulation (MAX19693)

The MAX19693 $f_{DAC}/2$ (or f_{CLK}) modulation mode can be enabled or disabled by connecting the MOD pin to 3.3V or to ground. The EV kit circuit provides jumper JU4 to configure the MOD pin. Refer to the MAX19693 IC data sheet for more details on the MOD pin. See Table 5 for jumper JU4 configuration.

Table 5. Modulation Configuration (JU4)

SHUNT POSITION	MOD PIN	MODULATION MODE
1-2	Connected to AVDD3.3	Enabled
2-3*	Connected to GND	Disabled

**Default position.*

Output Resistor Calibration

The EV kit circuit features an on-board µP supervisor (U2) to generate the CAL signal required to calibrate the integrated output termination resistors. At power-up, the supervisor applies a logic-high to the CAL pin 140ms after the final supply voltage is within its specified range. Pressing switch SW1 recalibrates the integrated termination resistors by creating a logic-low pulse on the CAL pin. The shunt on jumper JU8 can be removed to apply an external logic signal to pin 1 of jumper JU8 and initiate a CAL operation. See Table 6 for jumper JU8 configuration. Refer to the IC data sheet for details on the CAL operation.

Table 6. Calibration Configuration (JU8)

SHUNT POSITION	CAL PIN	EV KIT FUNCTION
Installed*	Connected to U2 $\overline{\text{RESET}}$ pin	Calibration initiated by µP supervisor U2
Not installed	Not connected	User-supplied logic signal at pin 1 of jumper JU8

**Default position.*

Input Register Scan (MAX19693)

The MAX19693 scan function can be enabled or disabled by configuring the SE pin. When the scan function is enabled, the contents of the input register are shifted out on the SO pin. Connect a digital sampling device to pin 1 of JU6 to access the scan output data on the SO pin. The EV kit circuit provides jumper JU7, which is used to enable or disable the scan function. During normal operation, install the shunt across jumper JU7 to disable the scan function. Refer to the MAX19693 IC data sheet for more details. See Table 7 for jumper JU7 configuration.

Table 7. Scan Configuration (JU7)

SHUNT POSITION	SE PIN	SCAN FUNCTION
Installed*	Connected to GND	Scan disabled
Not installed	Not connected (SE pin internally pulled down to ground GND)	User must supply a 1.8V CMOS logic signal to pin 1 of jumper JU7 to enable scan

**Default position.*

Using the HSDCEP Data Source Board with the EV Kit

The high-speed data converter evaluation platform (HSDCEP) can be used as a high-speed data source for the EV kit. Test patterns can be generated using a PC and uploaded to the HSDCEP for evaluation of the MAX19692 or MAX19693 EV kits. EV kit-specific firmware load is required to configure the HSDCEP. The most up-to-date firmware can be downloaded from www.maxim-ic.com/HSDCEP_Firmware. When loading the HSDCEP firmware for the DAC, select the appropriate firmware version based on the DAC's update rate (see Table 8). See Table 9 for EV kit jumper configuration when using the HSDCEP.

Table 8. Firmware Select

DAC UPDATE RATE	FIRMWARE VERSION
≥ 1Gsps	MAX19692_DDR_revYY.bit or MAX19693_DDR_revYY.bit
< 1Gsps	MAX19692slow_DDR_revYY.bit or MAX19693slow_DDR_revYY.bit

Refer to the HSDCEP data sheet for specifics on system requirements, software installation, loading configuration file, and data pattern file format.

Table 9. EV Kit Configuration for Use with the HSDCEP

JUMPER	SHUNT POSITION	EV KIT FUNCTION
JU3	2-3	No delay added to DATACLK
JU5	1-2	EV kit interface in DDR mode

Connecting the HSDCEP to the EV Kit

The HSDCEP and EV kit boards can be connected using the hardware supplied with the EV kit. See Figure 1 for details when connecting the boards together. Alternatively, the two boards can be connected with coaxial ribbon cables (Samtec, Part No. HQCD-060.00-STR-TBR-1). Note that it is necessary to use either the supplied hardware or cables to obtain a reliable electrical connection between the two boards.

Interfacing the EV Kit to a Pattern Generator

The EV kit provides QSH connectors (H1 and H2) to connect to Maxim's HSDCEP data source board. If the HSDCEP is not available, order the 12-bit LVDS adapter board (LVDSADPB12+) and connect it to connectors H1 and H2. Interface a 48-bit LVDS pattern generator to the 0.1in 2 x 24 headers (J1–J4) on the adapter board. The header data pins are labeled on the board with their appropriate data bit designation. Table 10 details header connections for J1 through J4. Use the labels on the LVDS adapter board or Table 10 to match the data bits from the pattern generator to the corresponding data pins on headers J1 through J4.

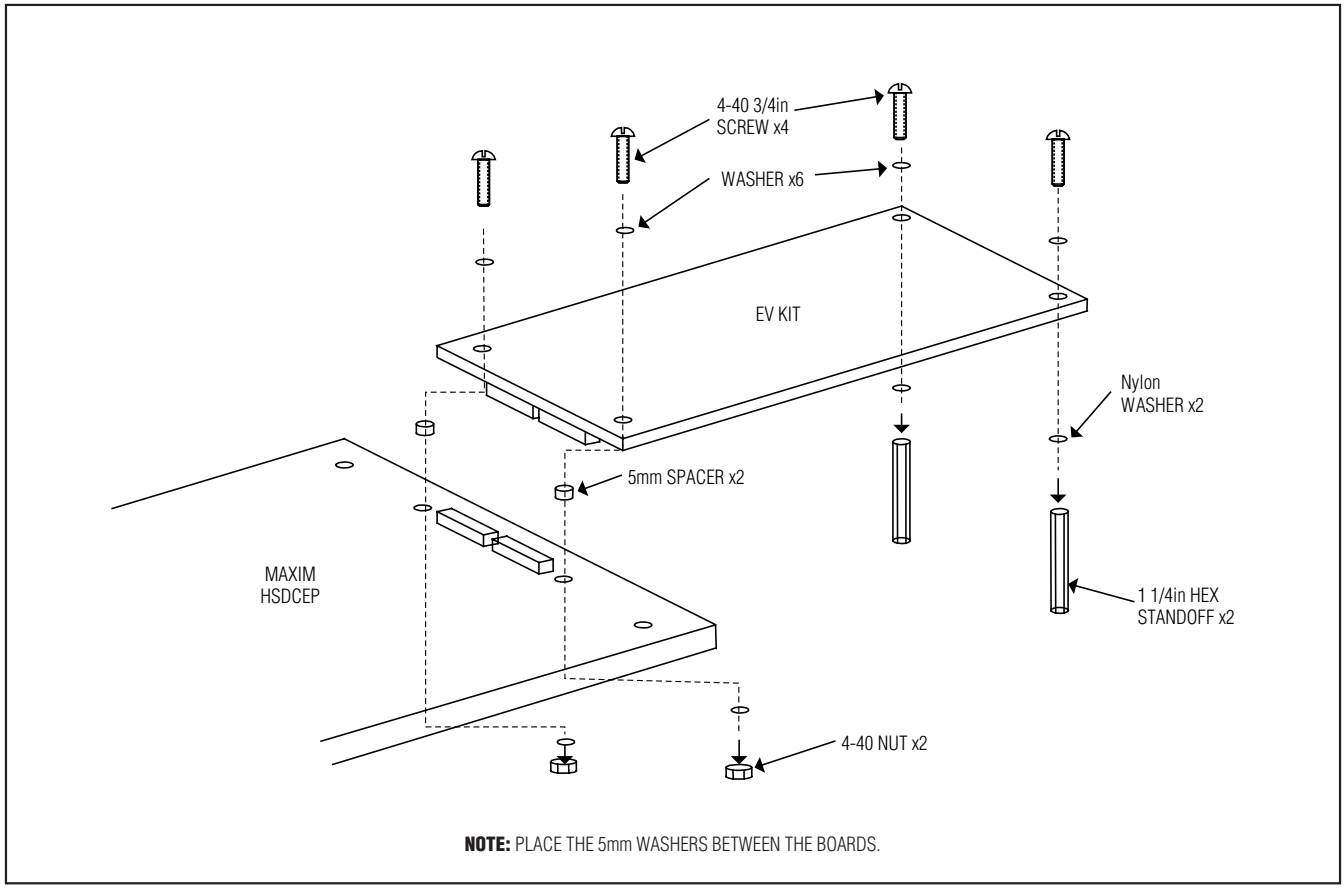

Figure 1. Connection of HSDCEP to MAX19692/MAX19693 EV Kits Using the Provided Hardware

Table 10. 12-Bit LVDS Adapter Board Digital Input Signals

CHANNEL A		CHANNEL B		CHANNEL C		CHANNEL D	
SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN
DAN0	J4-1	DBN0	J3-1	DCN0	J2-1	DDN0	J1-1
DAP0	J4-3	DBP0	J3-3	DCP0	J2-3	DDP0	J1-3
DAN1	J4-5	DBN1	J3-5	DCN1	J2-5	DDN1	J1-5
DAP1	J4-7	DBP1	J3-7	DCP1	J2-7	DDP1	J1-7
DAN2	J4-9	DBN2	J3-9	DCN2	J2-9	DDN2	J1-9
DAP2	J4-11	DBP2	J3-11	DCP2	J2-11	DDP2	J1-11
DAN3	J4-13	DBN3	J3-13	DCN3	J2-13	DDN3	J1-13
DAP3	J4-15	DBP3	J3-15	DCP3	J2-15	DDP3	J1-15
DAN4	J4-17	DBN4	J3-17	DCN4	J2-17	DDN4	J1-17
DAP4	J4-19	DBP4	J3-19	DCP4	J2-19	DDP4	J1-19
DAN5	J4-21	DBN5	J3-21	DCN5	J2-21	DDN5	J1-21
DAP5	J4-23	DBP5	J3-23	DCP5	J2-23	DDP5	J1-23
DAN6	J4-25	DBN6	J3-25	DCN6	J2-25	DDN6	J1-25
DAP6	J4-27	DBP6	J3-27	DCP6	J2-27	DDP6	J1-27
DAN7	J4-29	DBN7	J3-29	DCN7	J2-29	DDN7	J1-29
DAP7	J4-31	DBP7	J3-31	DCP7	J2-31	DDP7	J1-31
DAN8	J4-33	DBN8	J3-33	DCN8	J2-33	DDN8	J1-33
DAP8	J4-35	DBP8	J3-35	DCP8	J2-35	DDP8	J1-35
DAN9	J4-37	DBN9	J3-37	DCN9	J2-37	DDN9	J1-37
DAP9	J4-39	DBP9	J3-39	DCP9	J2-39	DDP9	J1-39
DAN10	J4-41	DBN10	J3-41	DCN10	J2-41	DDN10	J1-41
DAP10	J4-43	DBP10	J3-43	DCP10	J2-43	DDP10	J1-43
DAN11	J4-45	DBN11	J3-45	DCN11	J2-45	DDN11	J1-45
DAP11	J4-47	DBP11	J3-47	DCP11	J2-47	DDP11	J1-47

Note: *All other pins are connected to ground.*

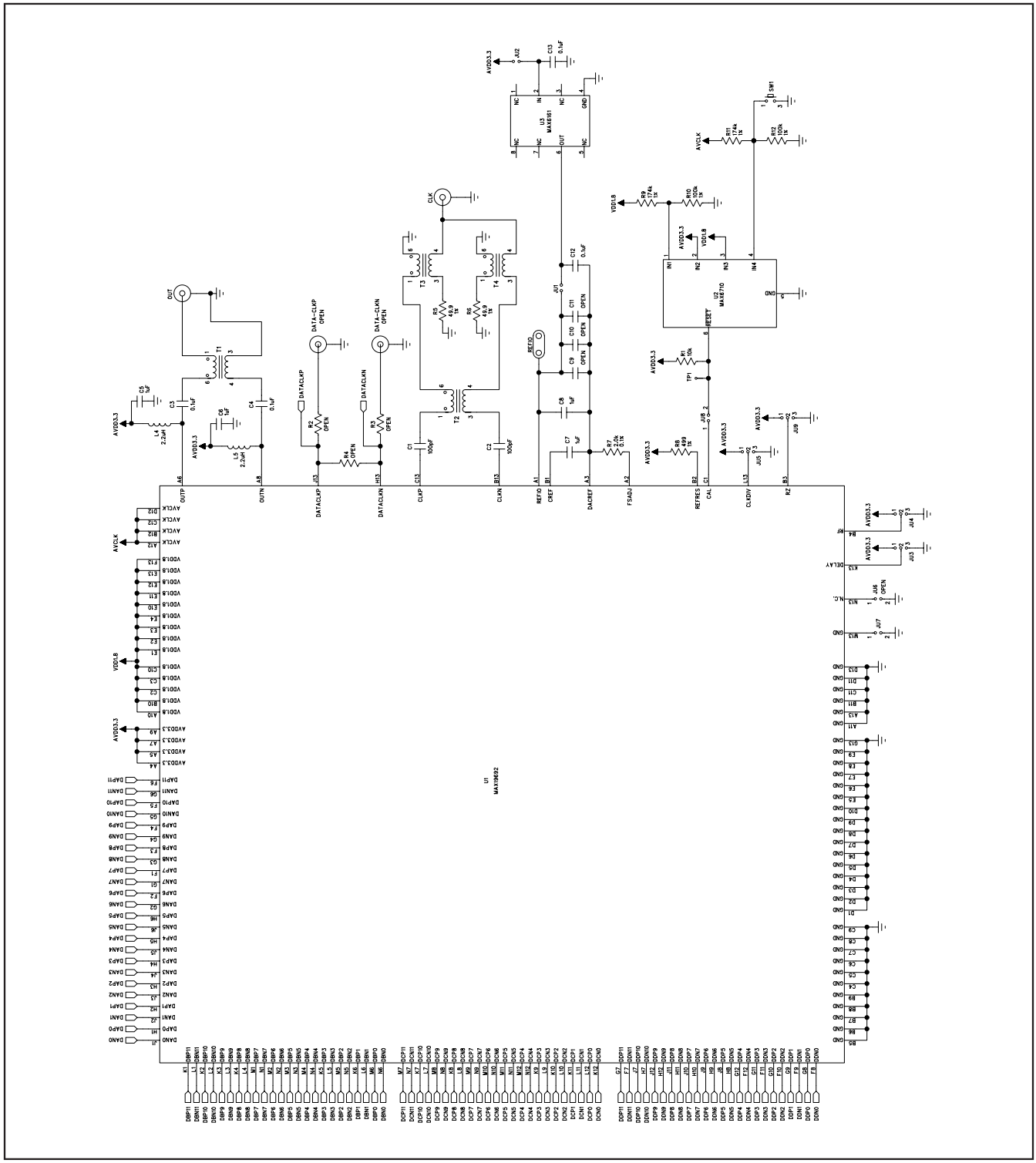

Figure 2a. MAX19692 EV Kit Schematic (Sheet 1 of 2)

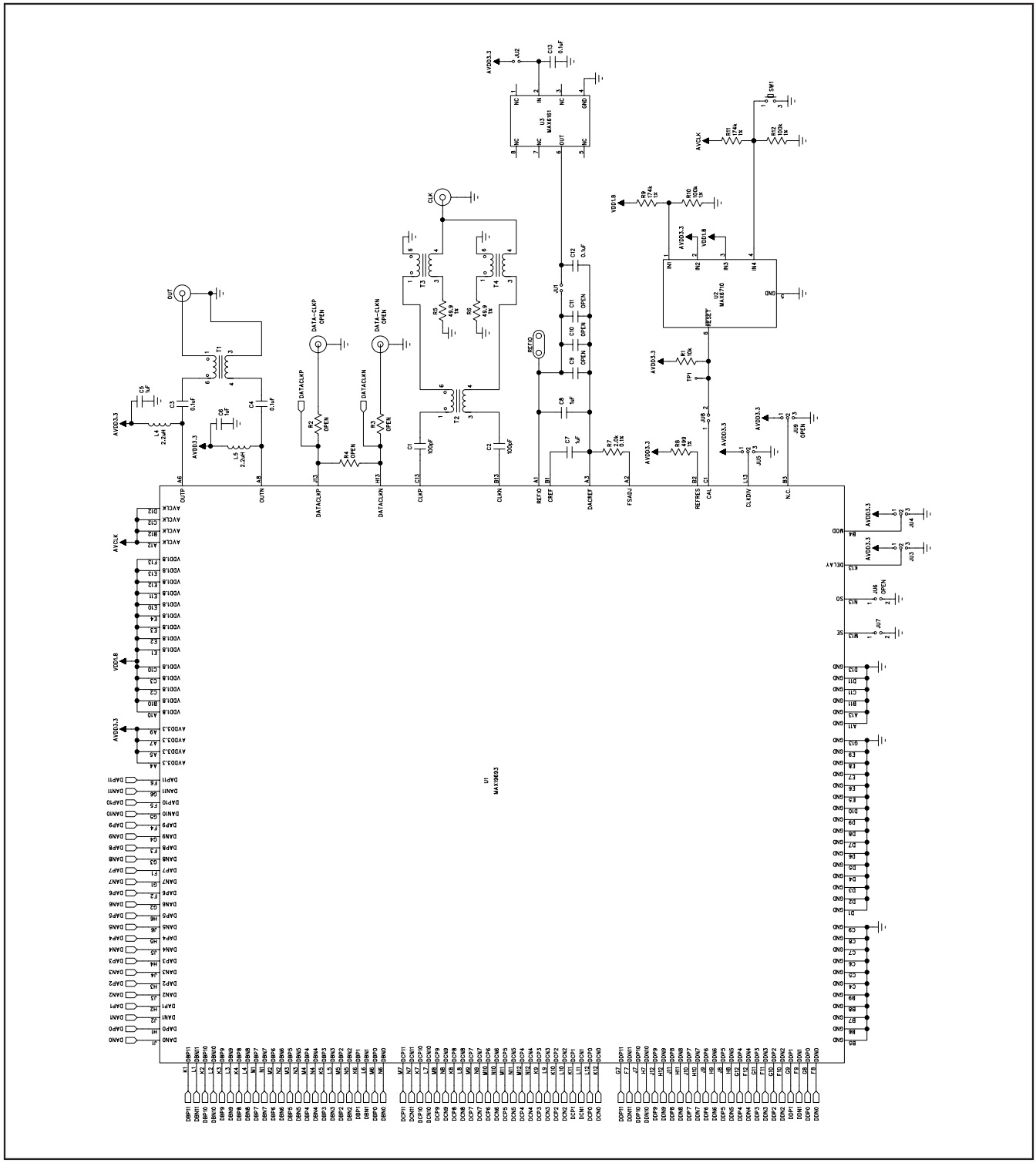

Figure 2b. MAX19693 EV Kit Schematic (Sheet 1 of 2)

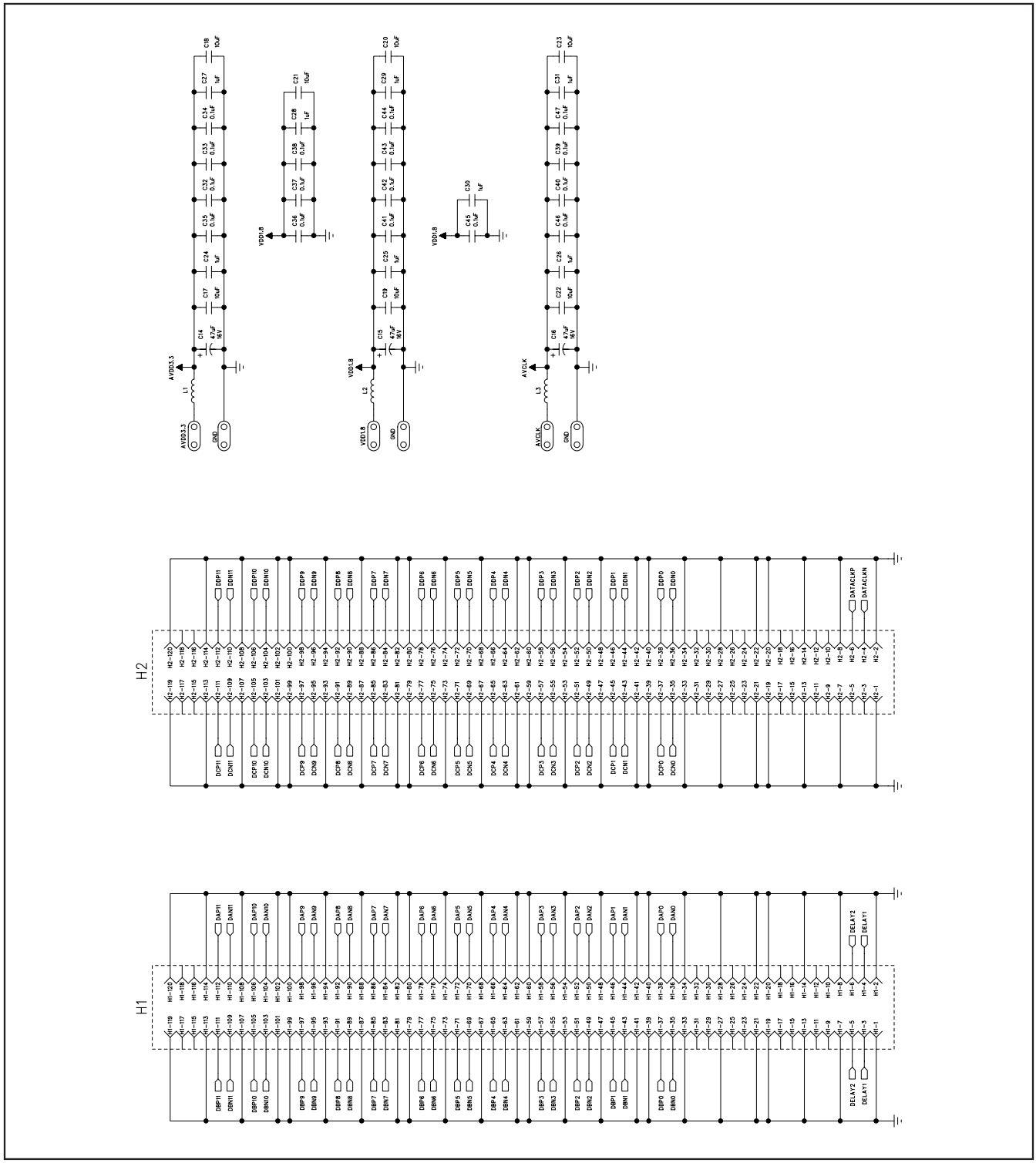

Figure 2c. MAX19692/MAX19693 EV Kit Schematic (Sheet 2 of 2)

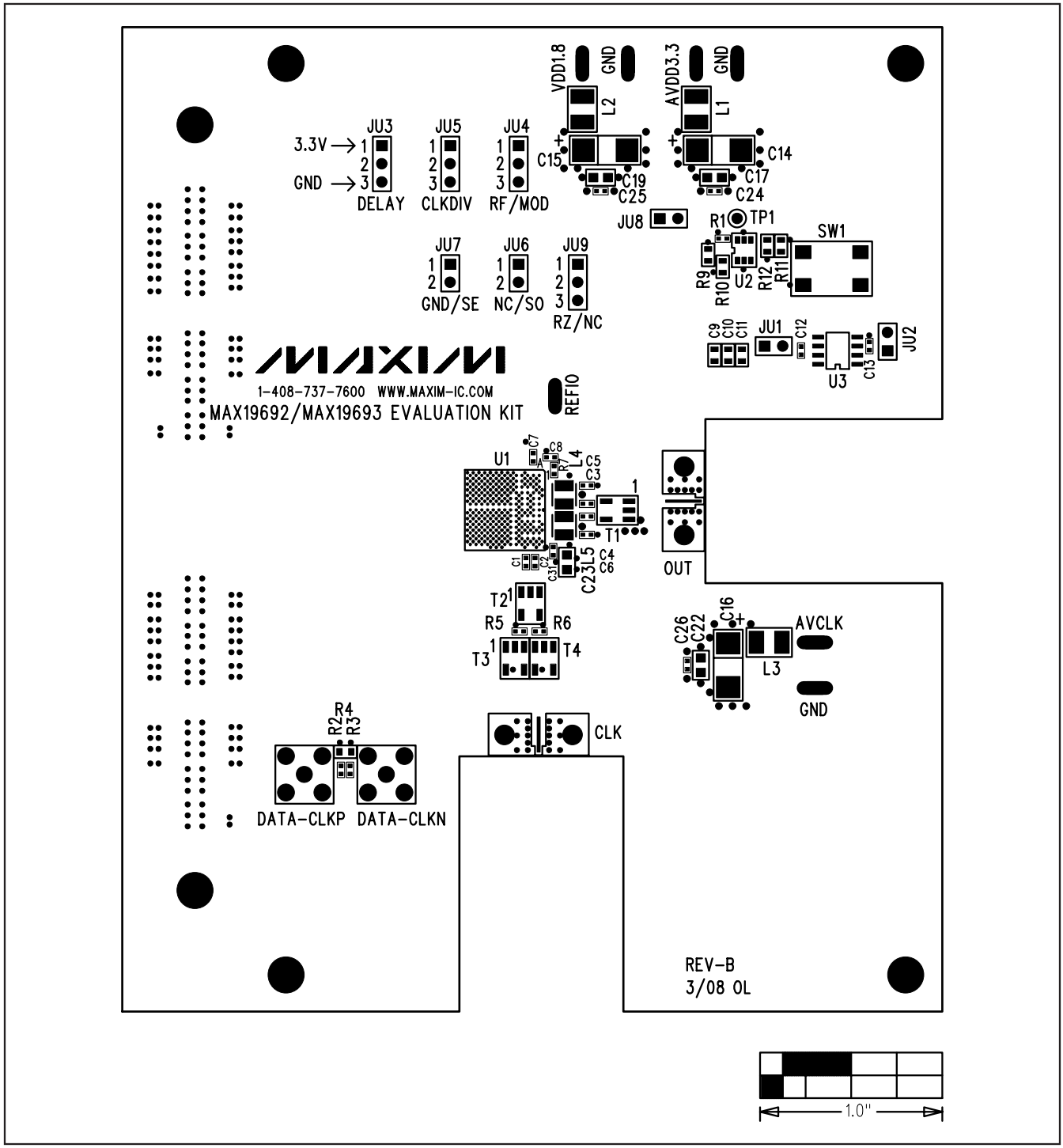

Figure 3. MAX19692/MAX19693 EV Kit Component Placement Guide—Component Side

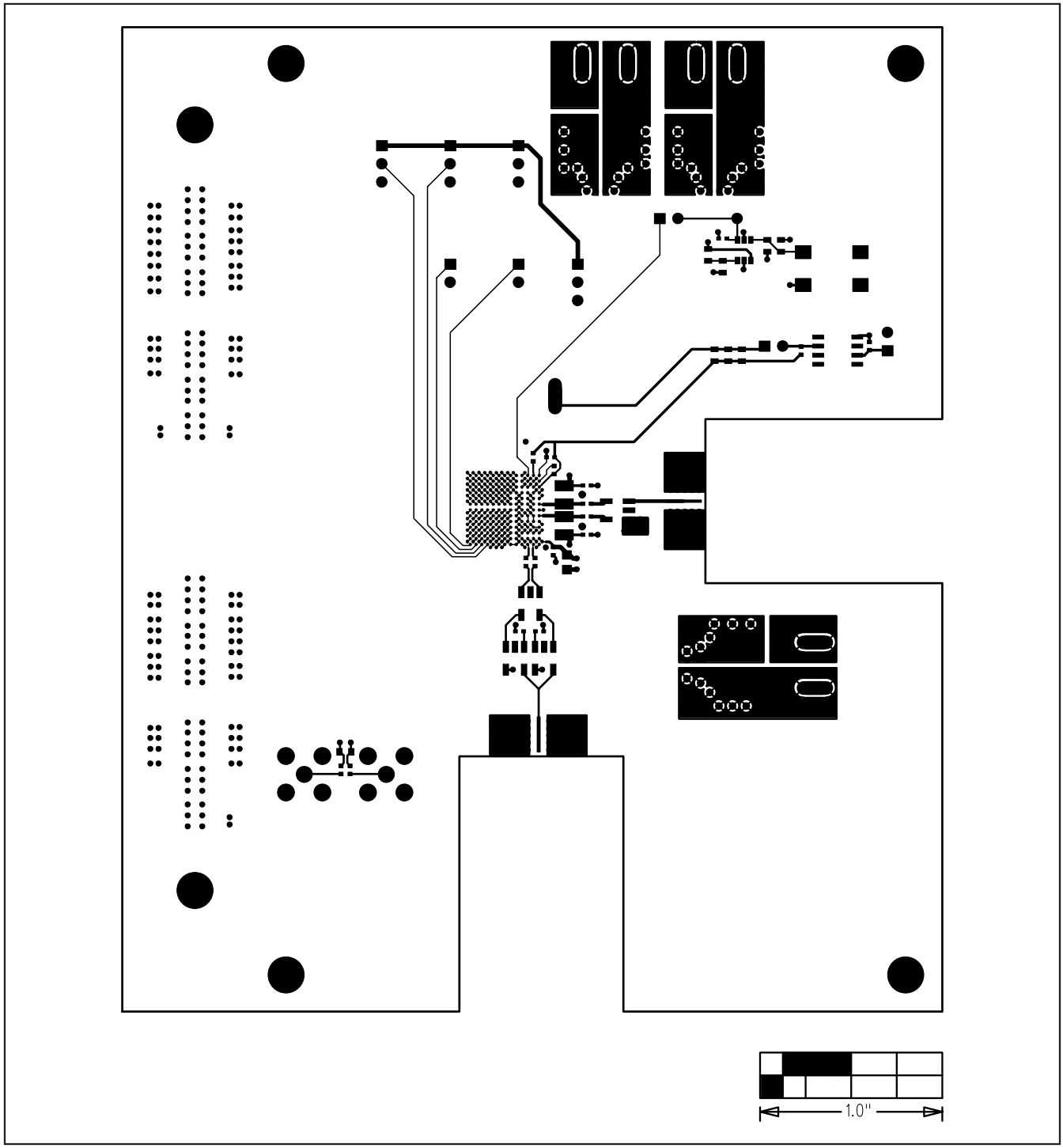

Figure 4. MAX19692/MAX19693 EV Kit PCB Layout—Component Side

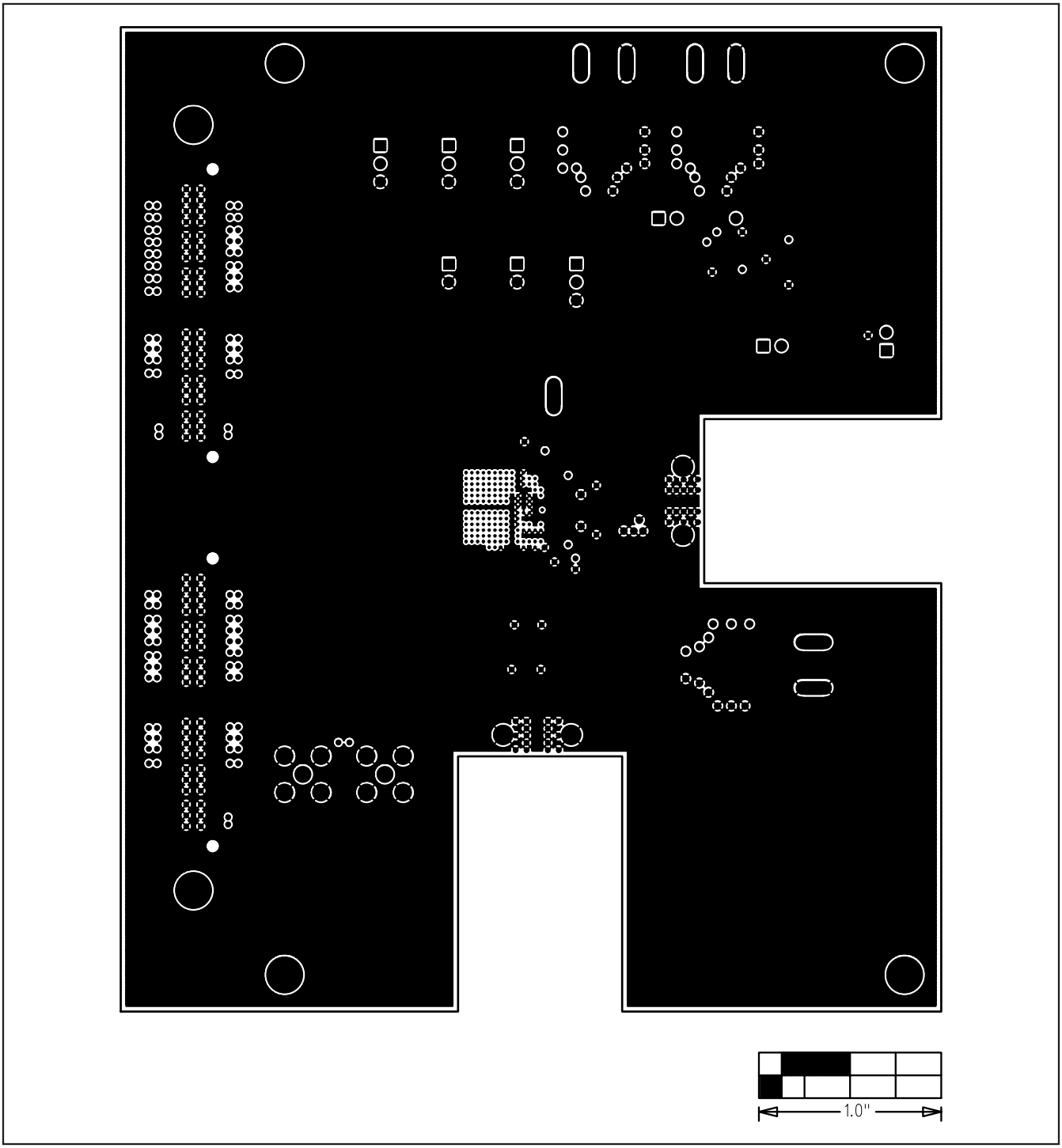

Figure 5. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 2)—Ground Plane

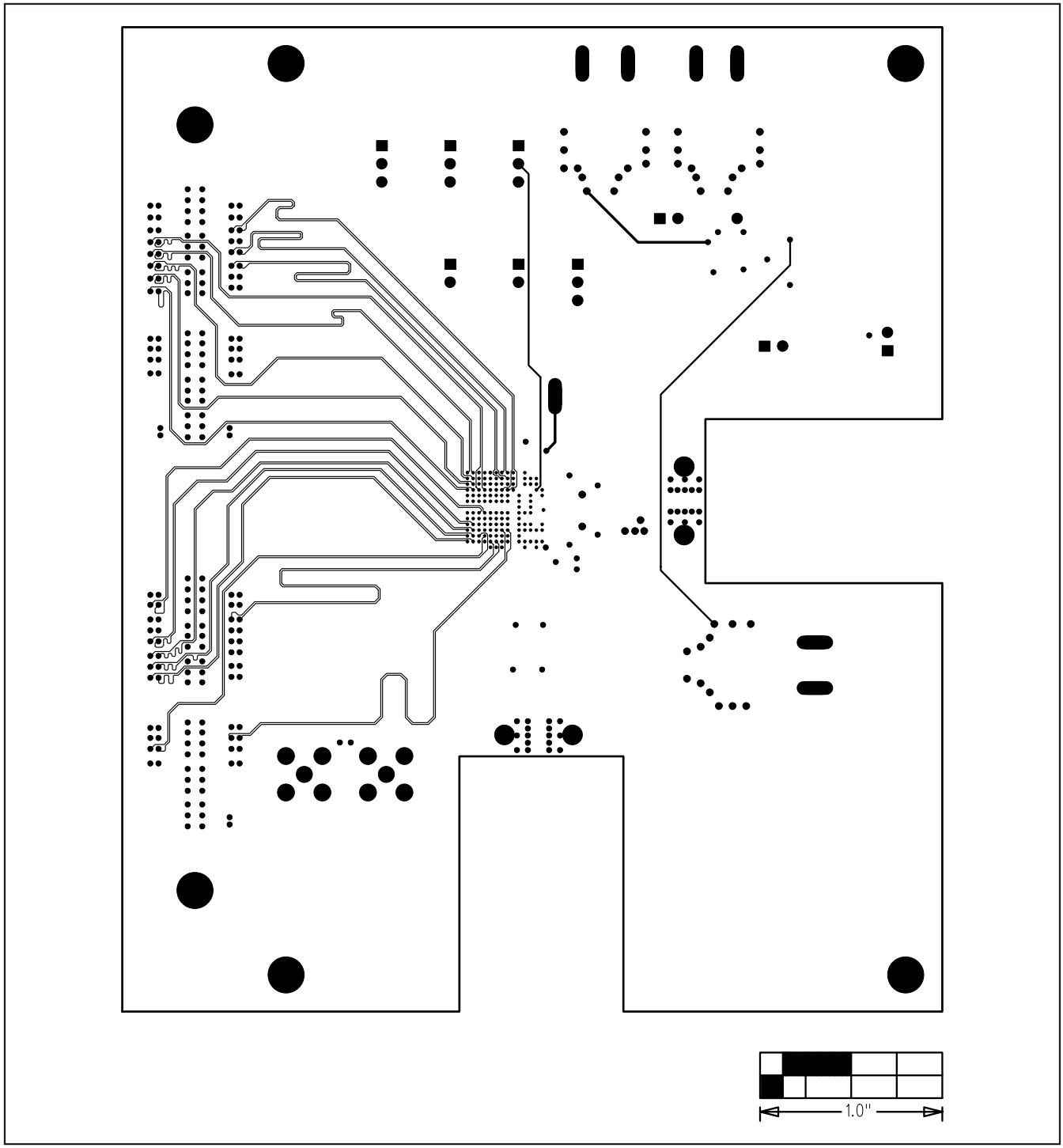

Figure 6. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 3)—Signals

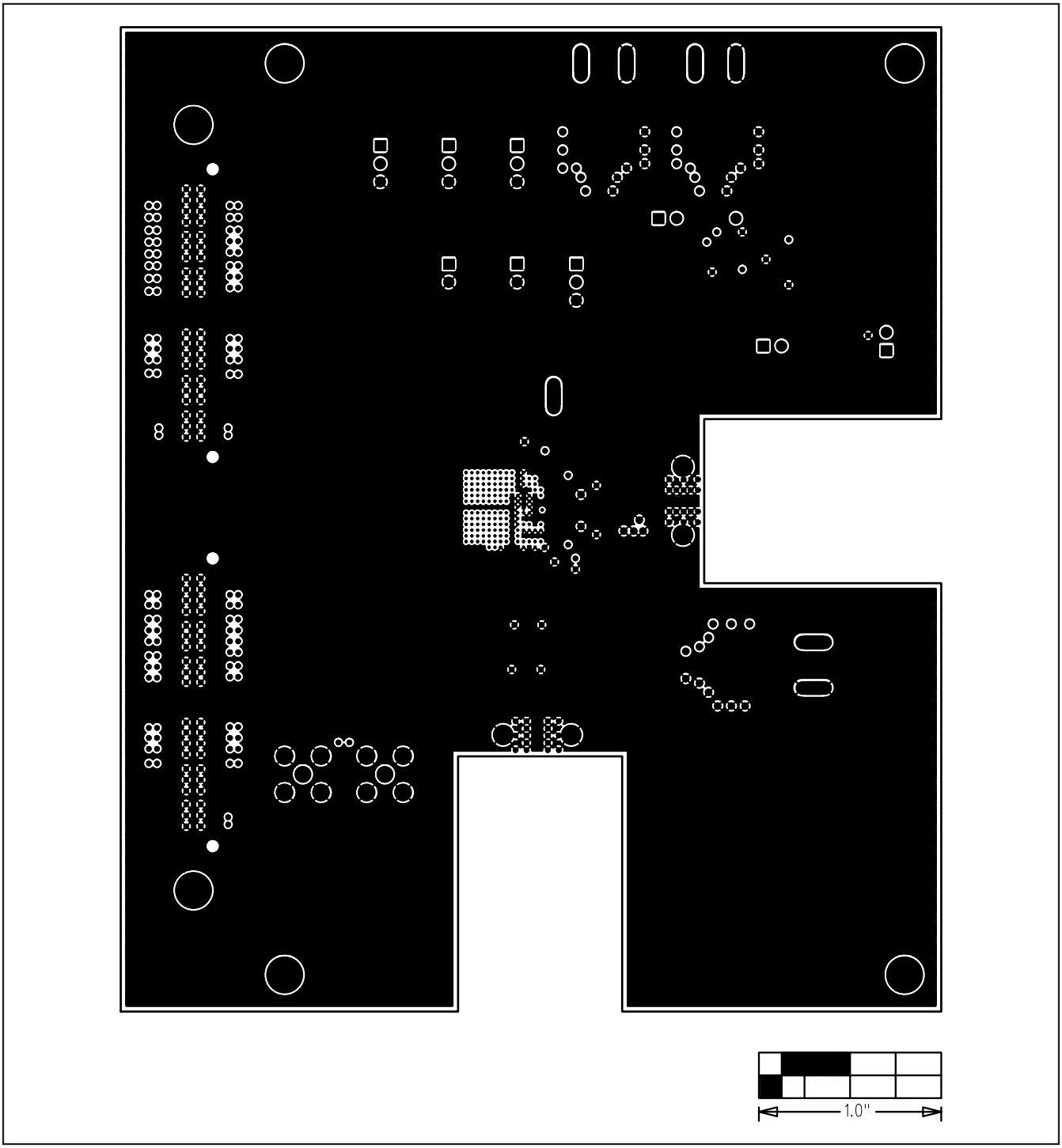

Figure 7. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 4)—Ground Plane

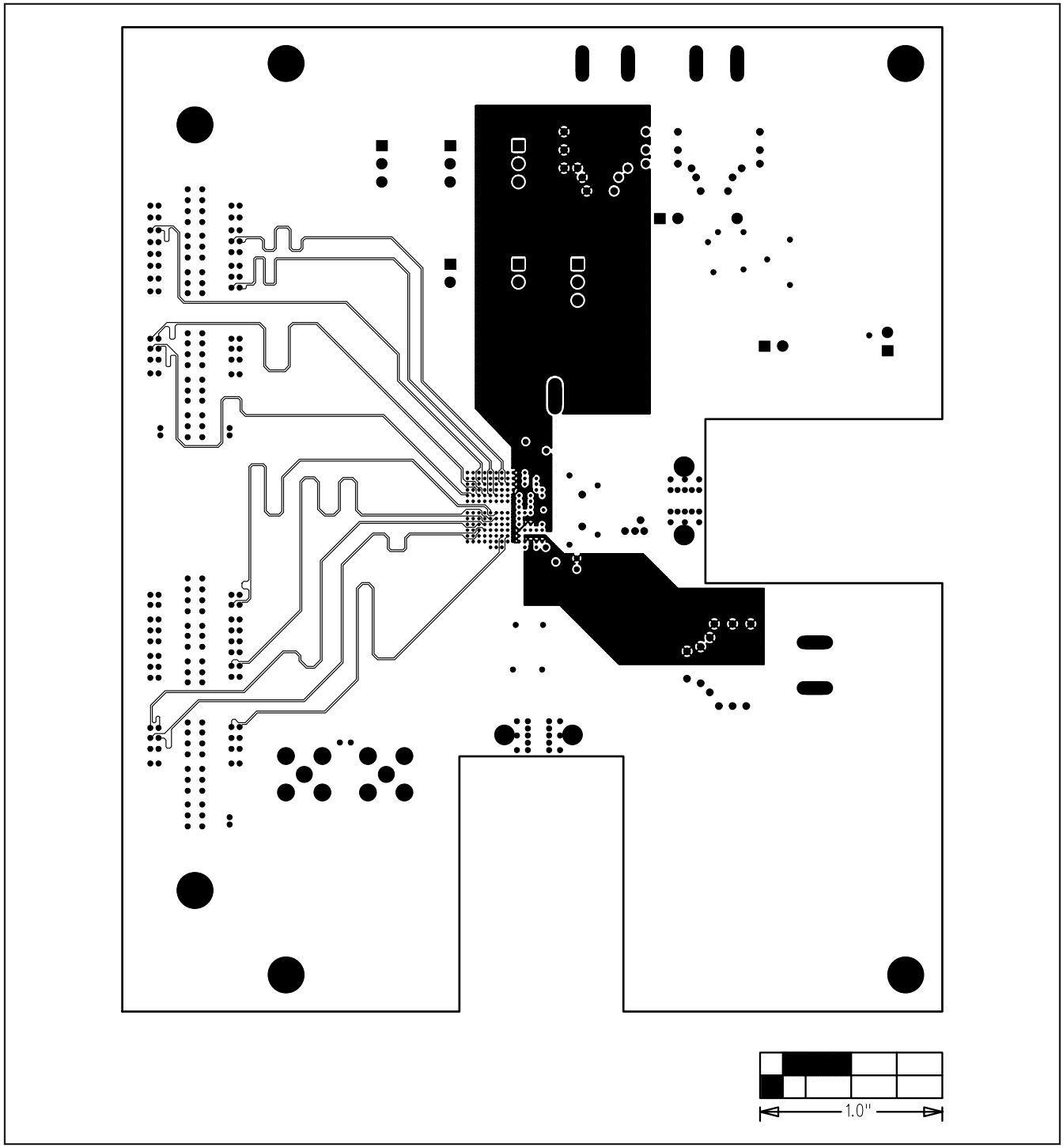

Figure 8. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 5)—Signals

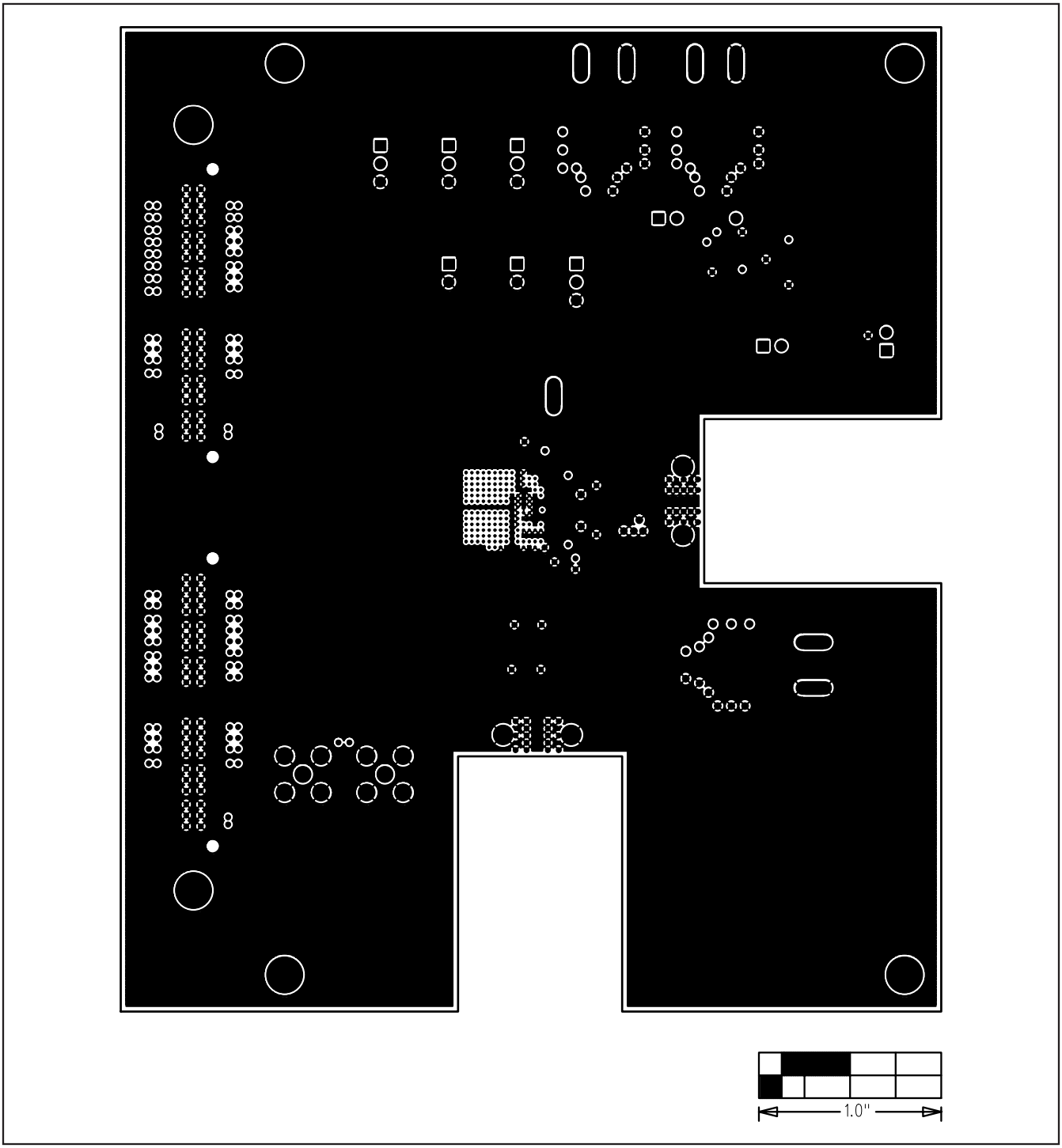

Figure 9. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 6)—Ground Plane

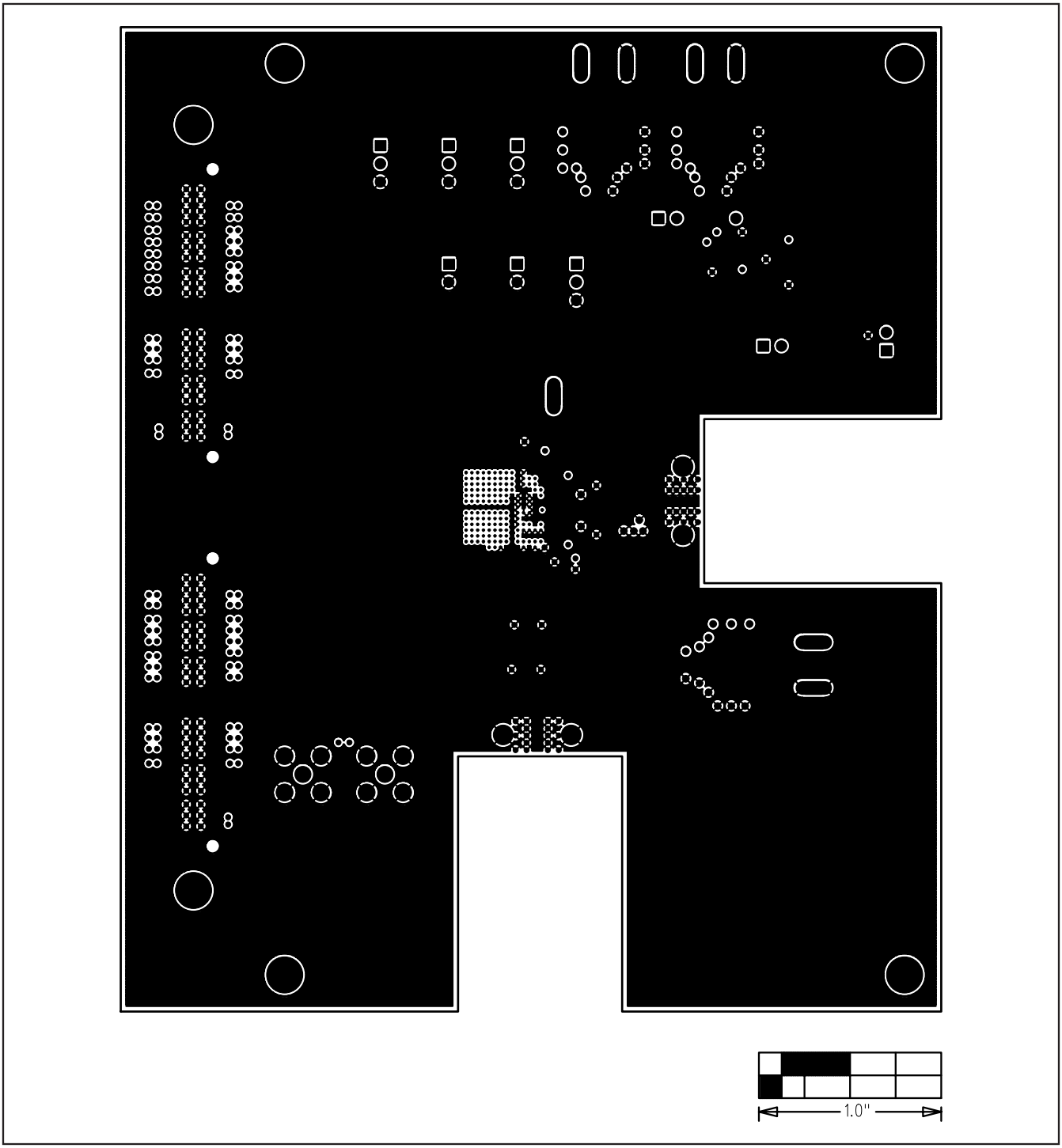

Figure 10. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 7)—Ground Plane

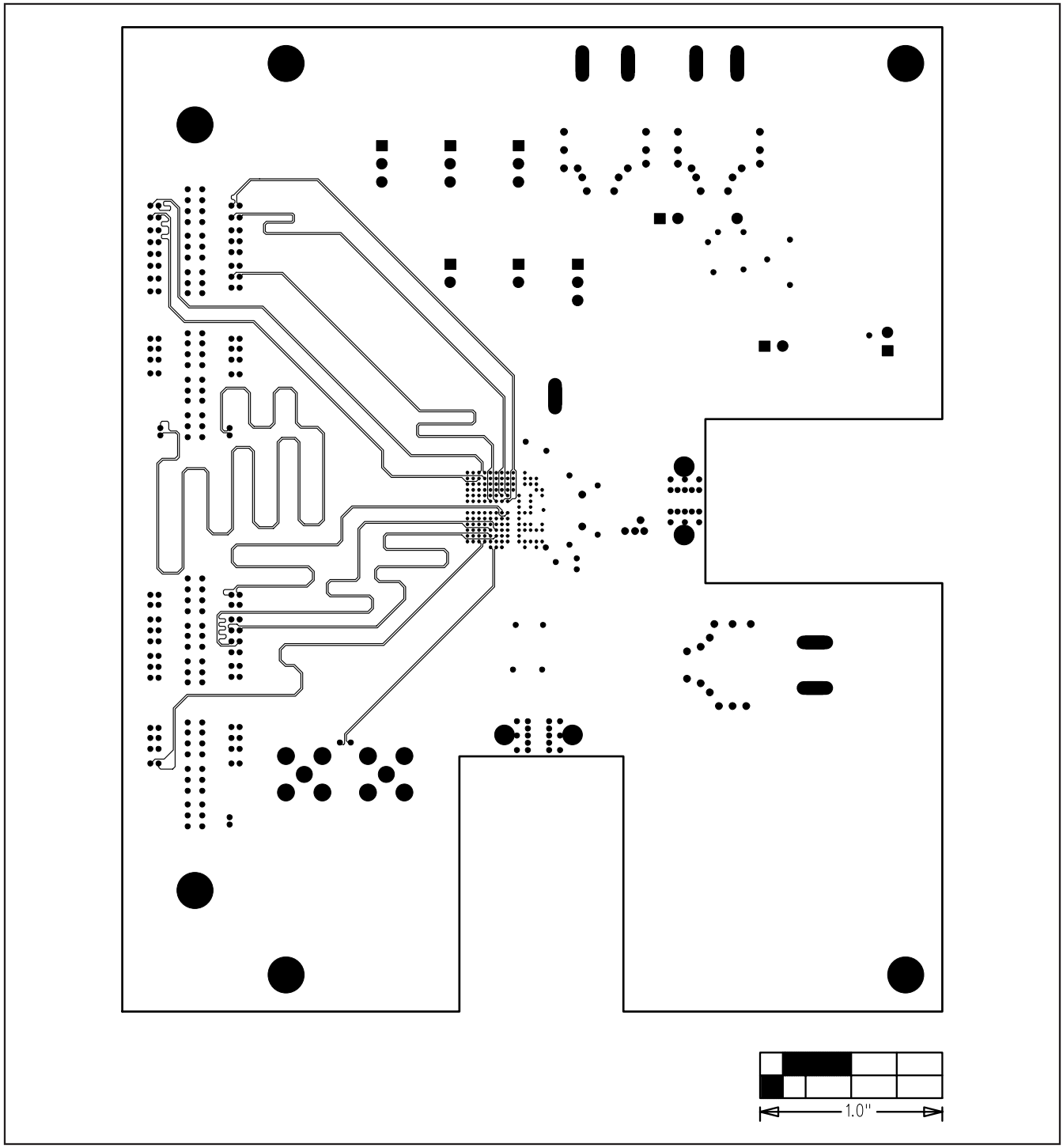

Figure 11. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 8)—Signals

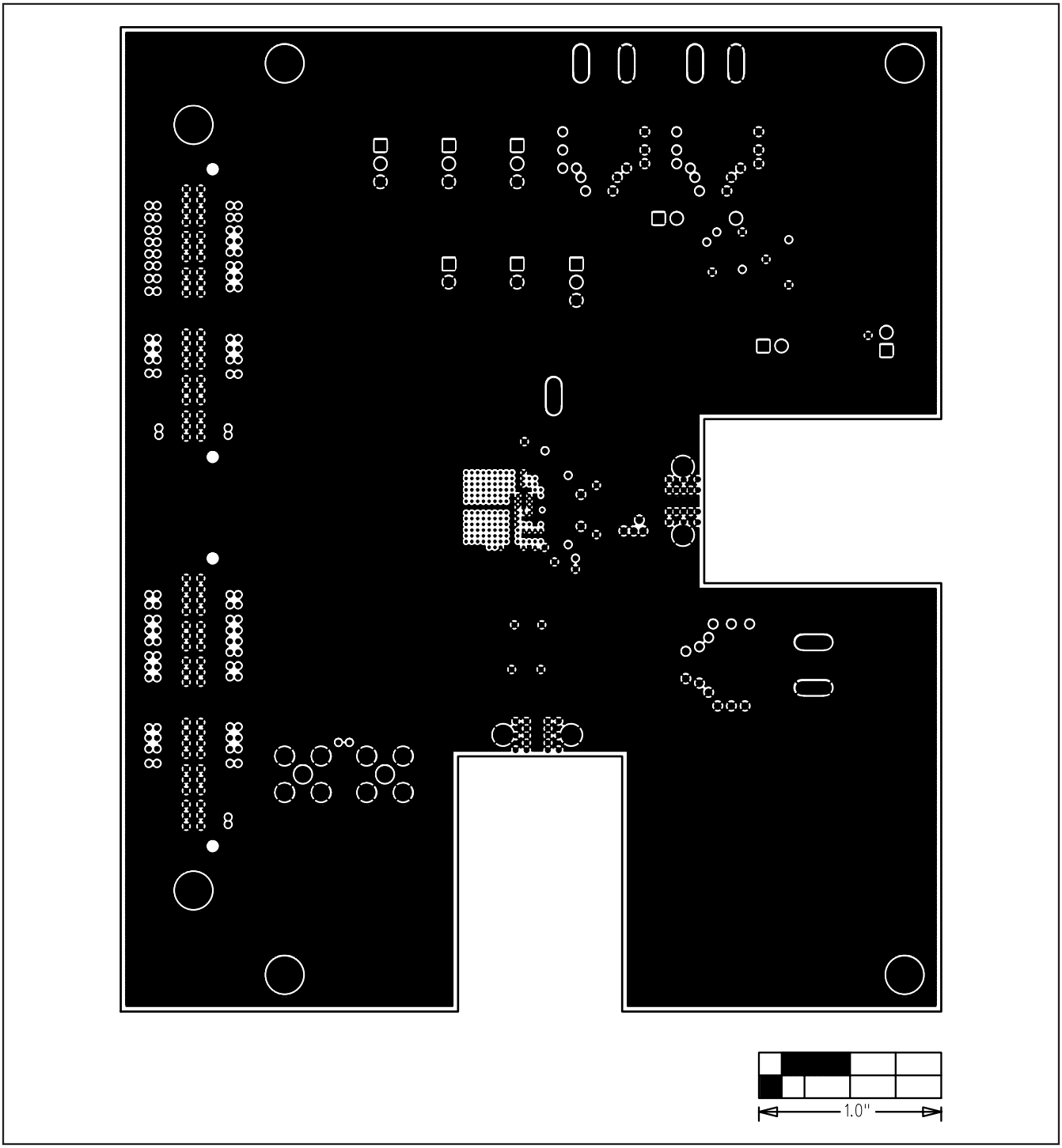

Figure 12. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 9)—Ground Plane

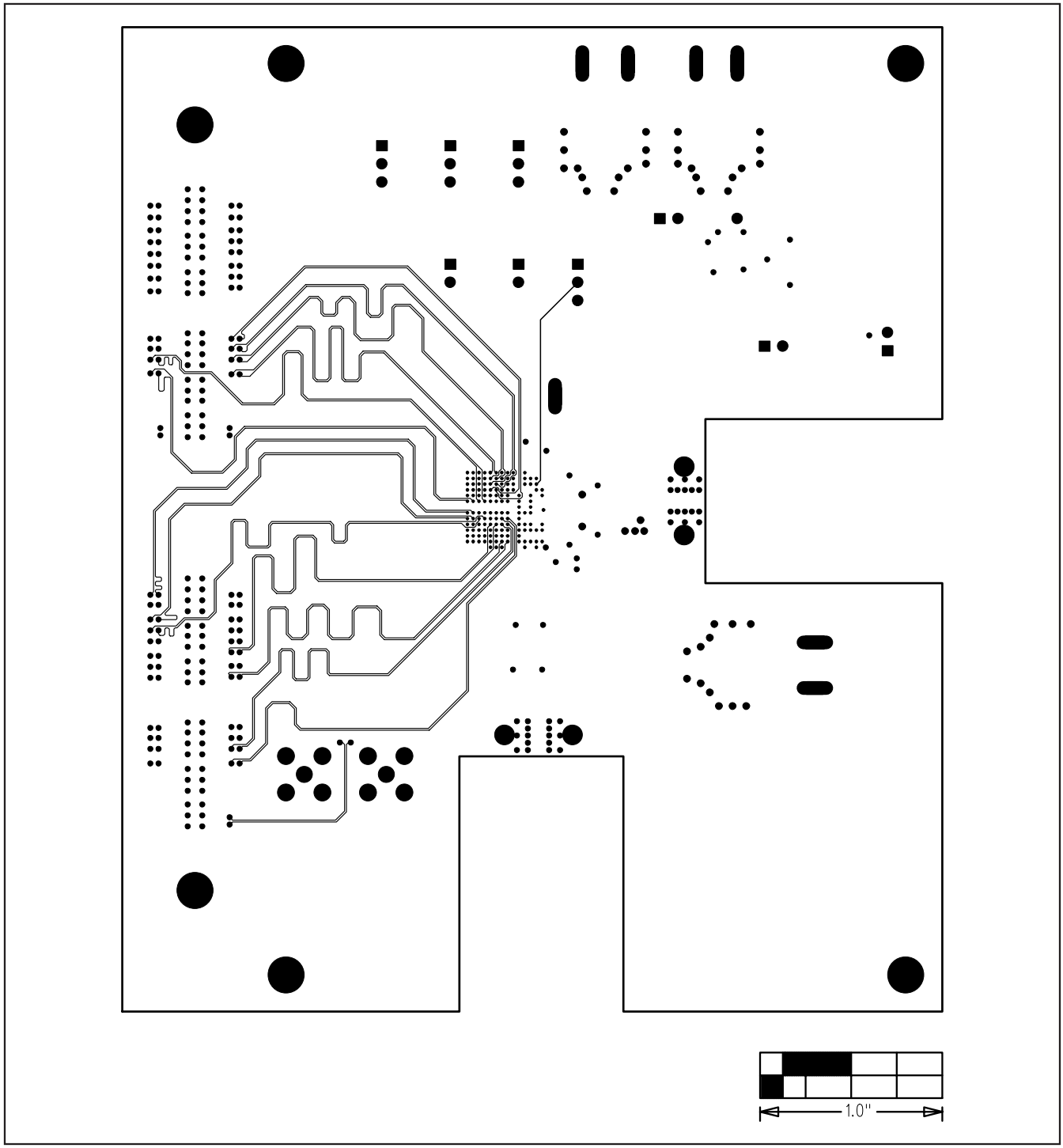

Figure 13. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 10)—Signals

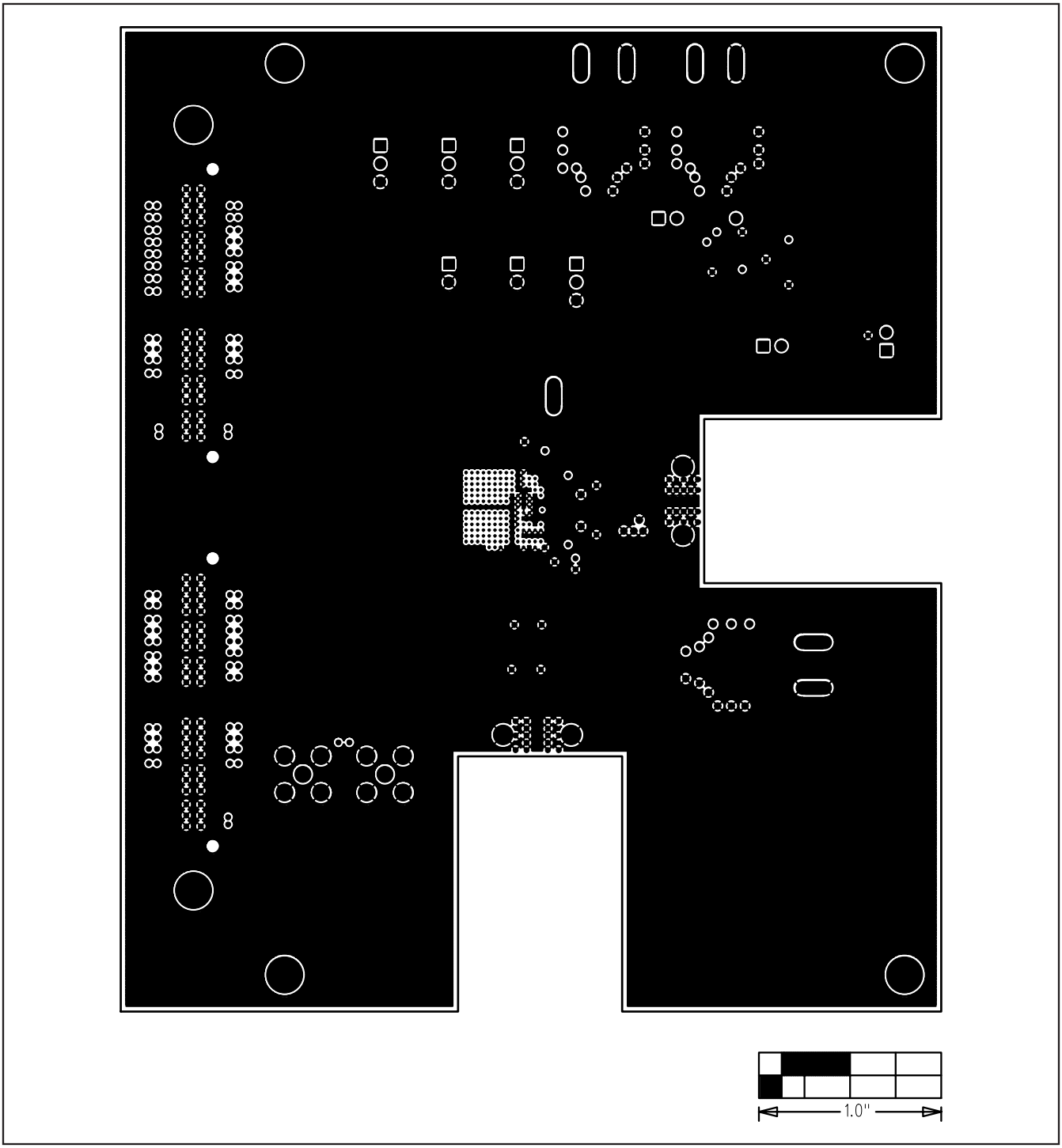

Figure 14. MAX19692/MAX19693 EV Kit PCB Layout (Inner Layer 11)—Ground Plane

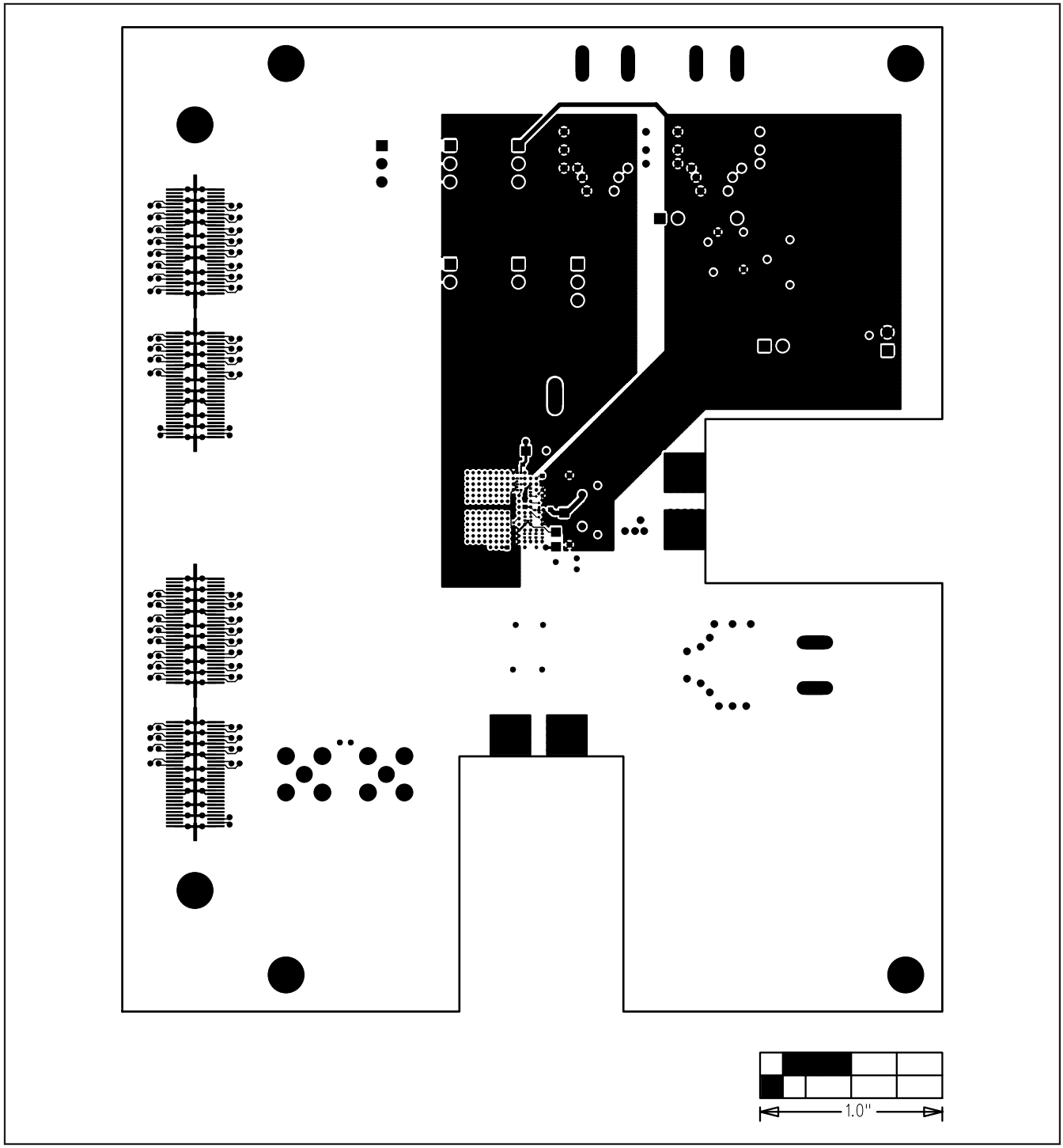

Figure 15. MAX19692/MAX19693 EV Kit PCB Layout—Solder Side

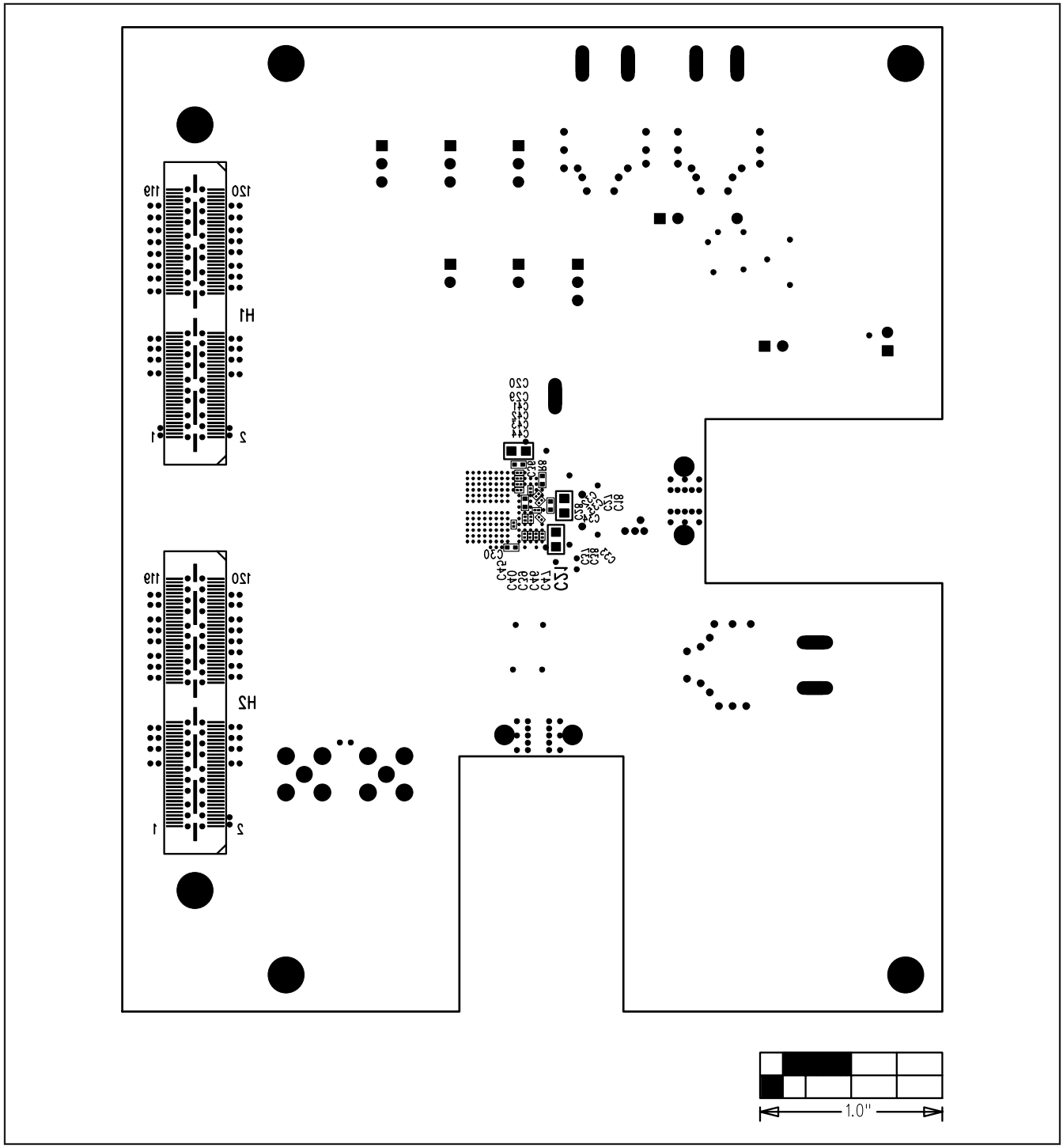

Figure 16. MAX19692/MAX19693 EV Kit Component Placement Guide—Solder Side

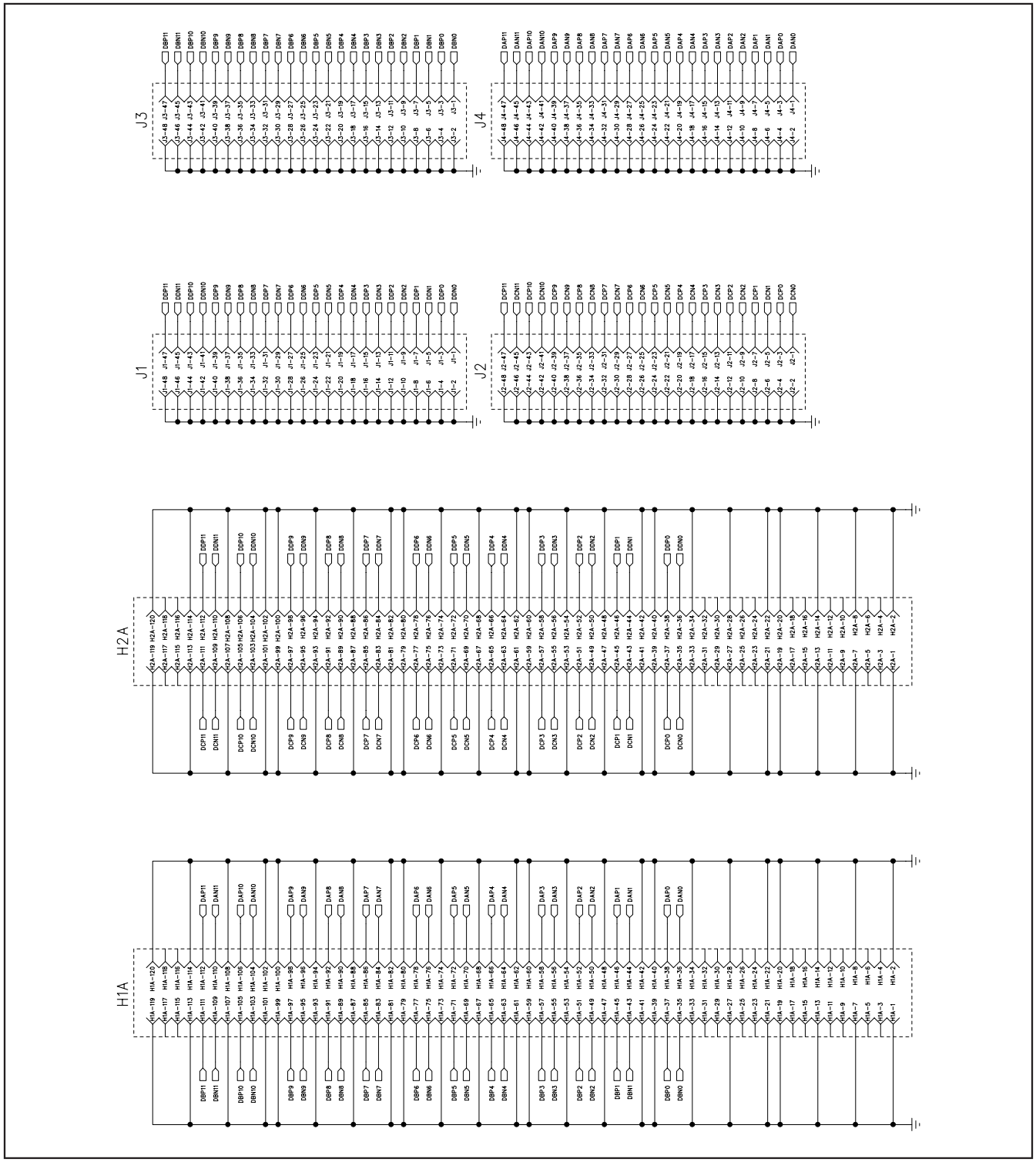

Figure 17. 12-Bit LVDS Adapter Board Schematic

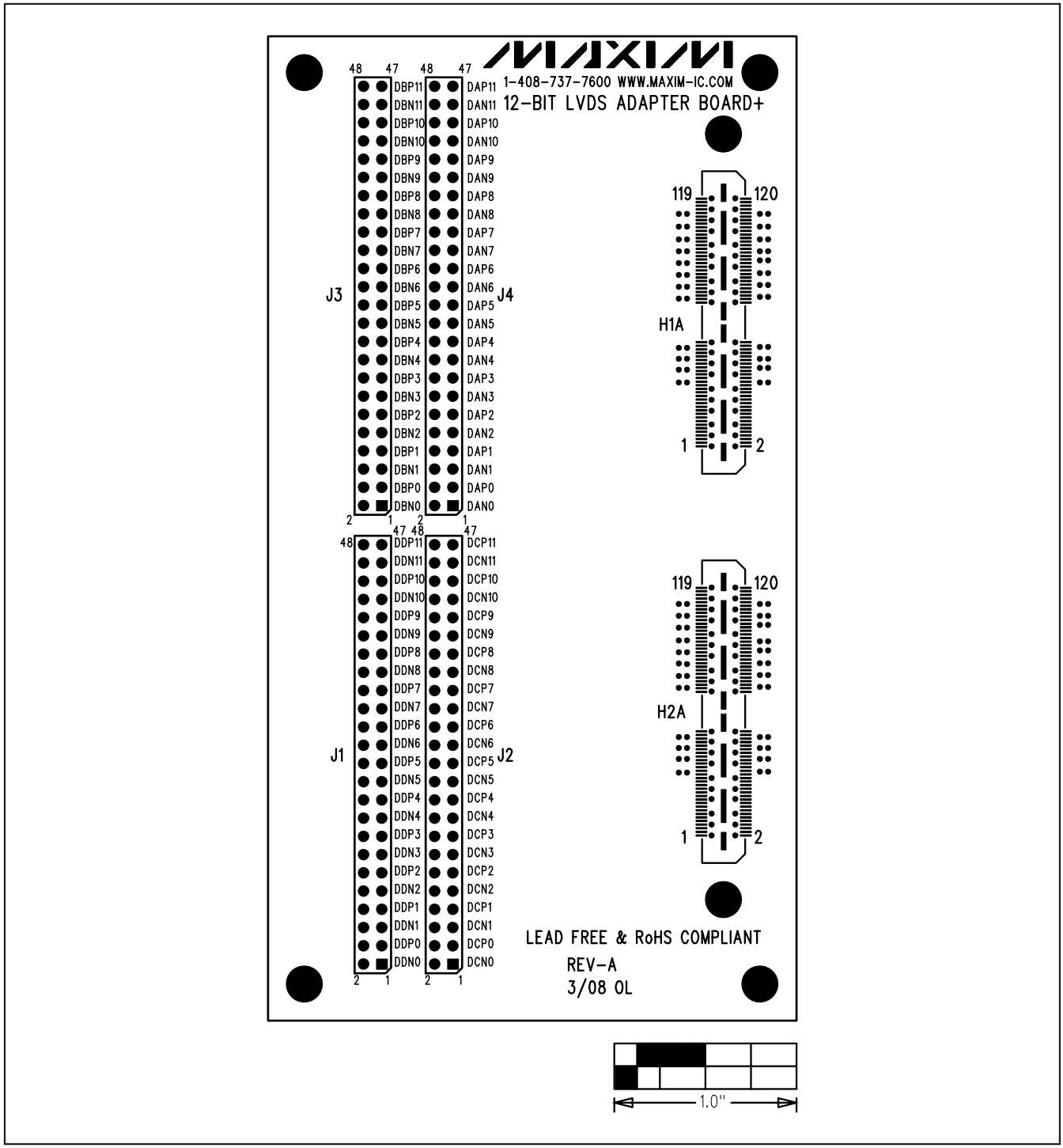

Figure 18. 12-Bit LVDS Adapter Board Component Placement Guide—Component Side

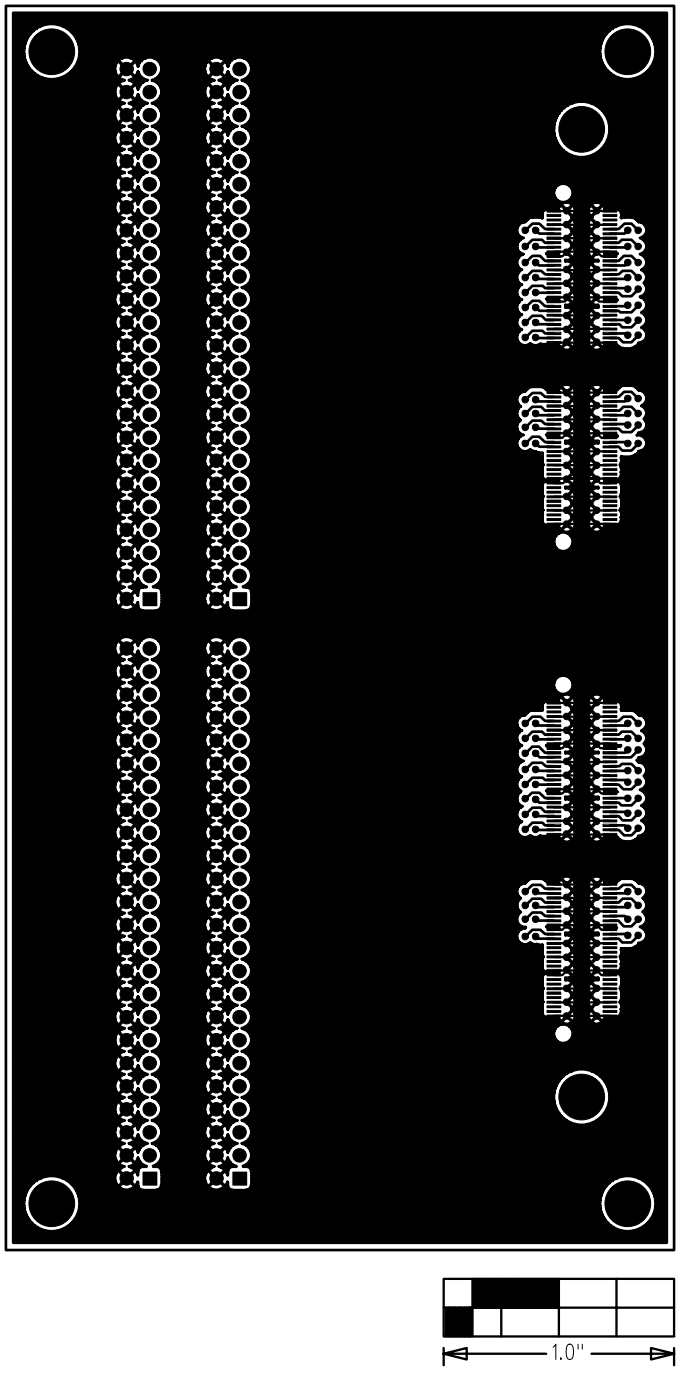

Figure 19. 12-Bit LVDS Adapter Board Layout—Component Side

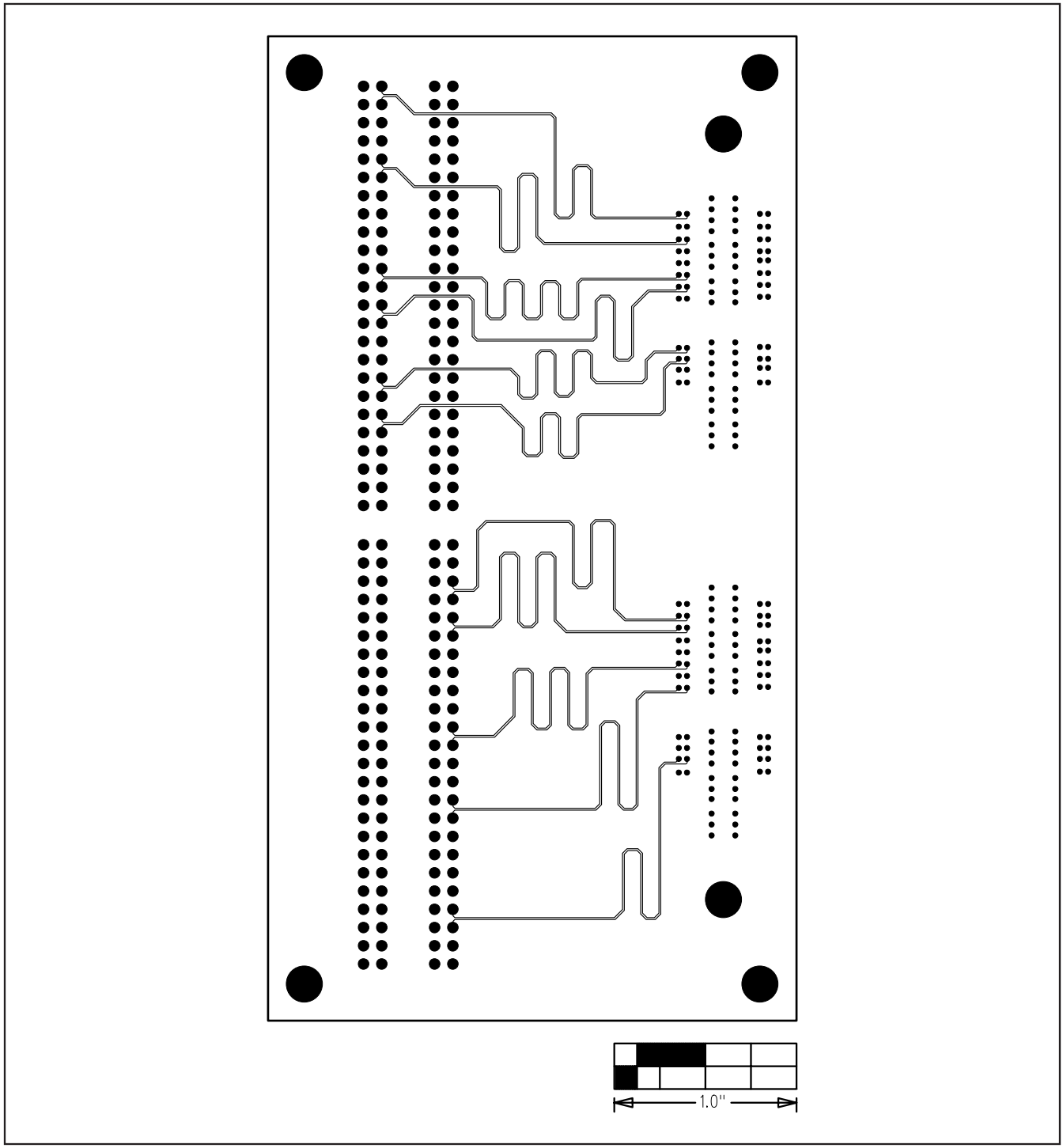

Figure 20. 12-Bit LVDS Adapter Board Layout (Inner Layer 2)—Signals

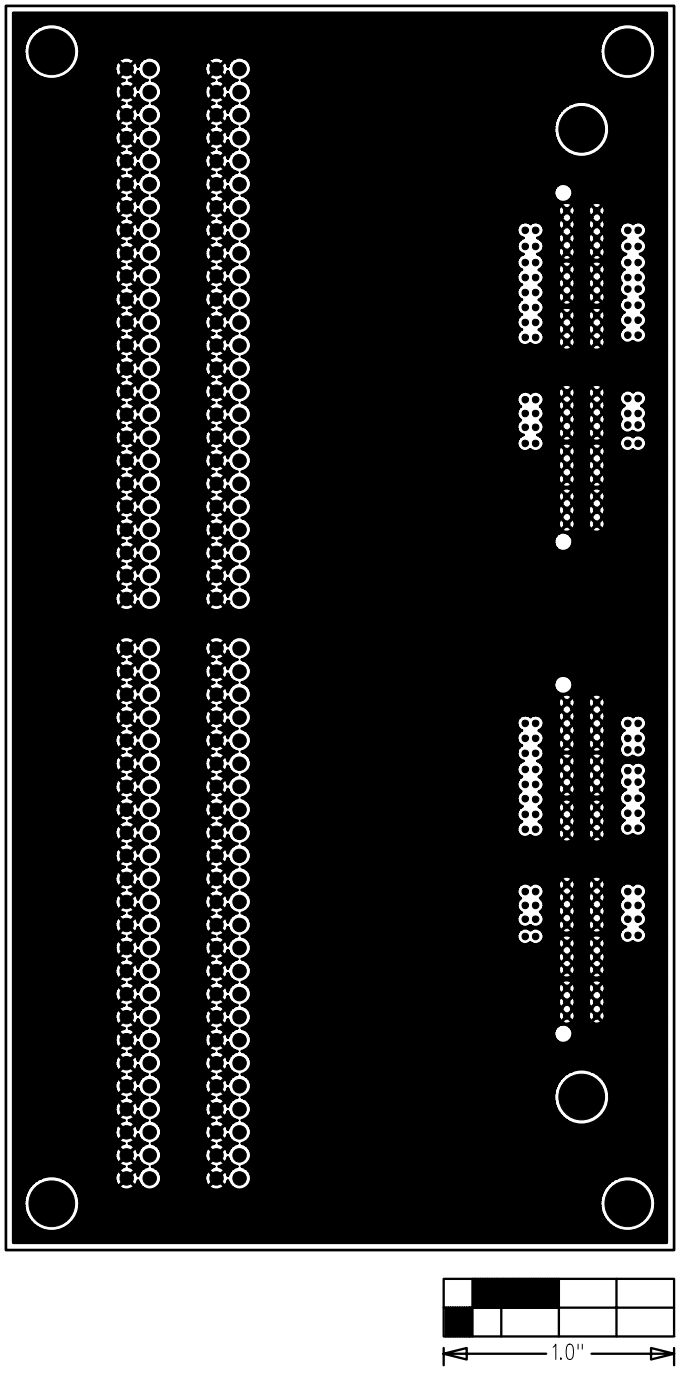

Figure 21. 12-Bit LVDS Adapter Board Layout (Inner Layer 3)—Ground Plane

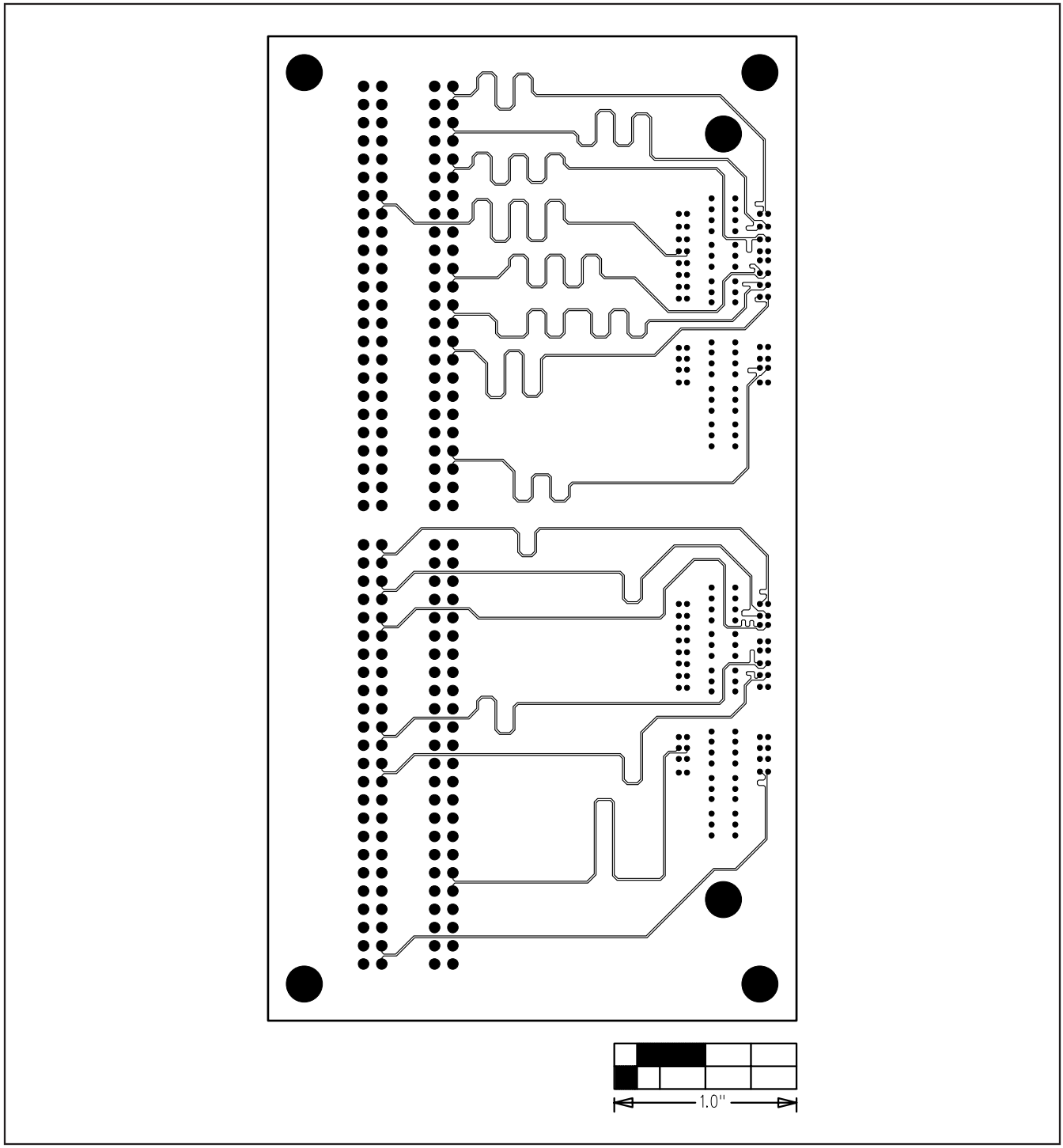

Figure 22. 12-Bit LVDS Adapter Board Layout (Inner Layer 4)—Signals

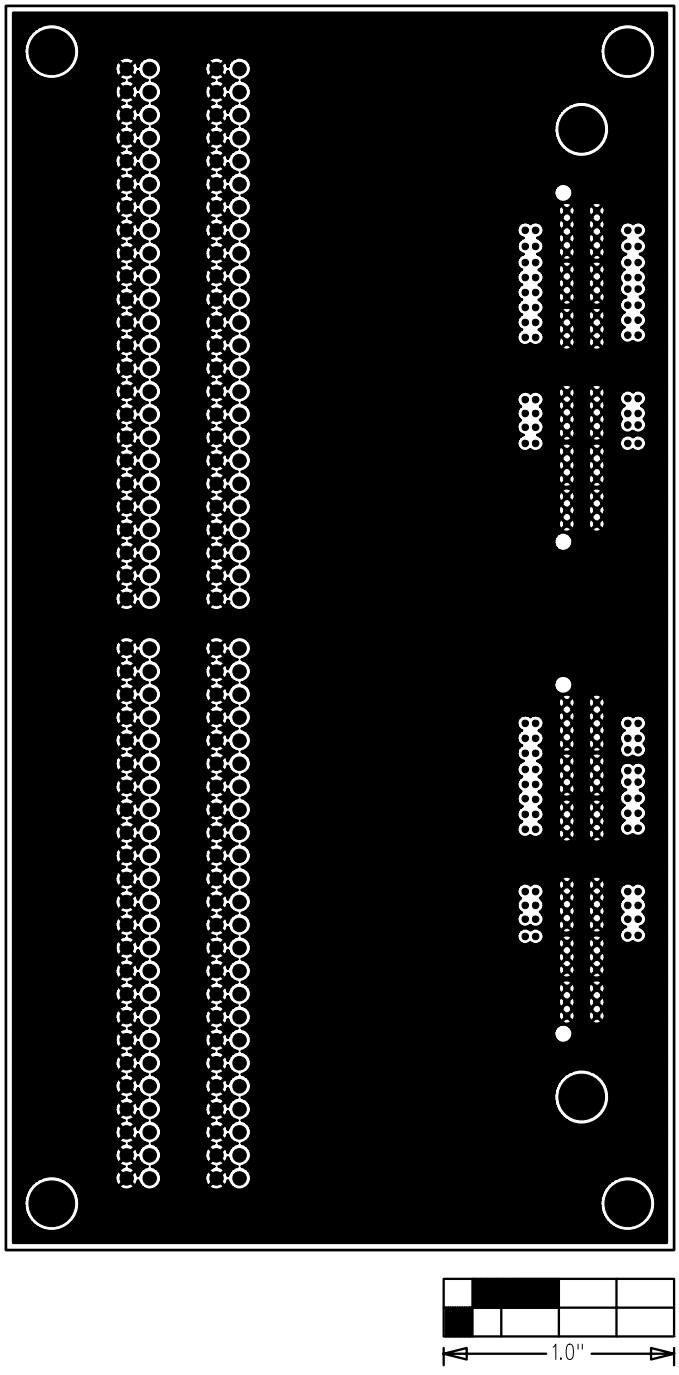

Figure 23. 12-Bit LVDS Adapter Board Layout (Inner Layer 5)—Ground Plane

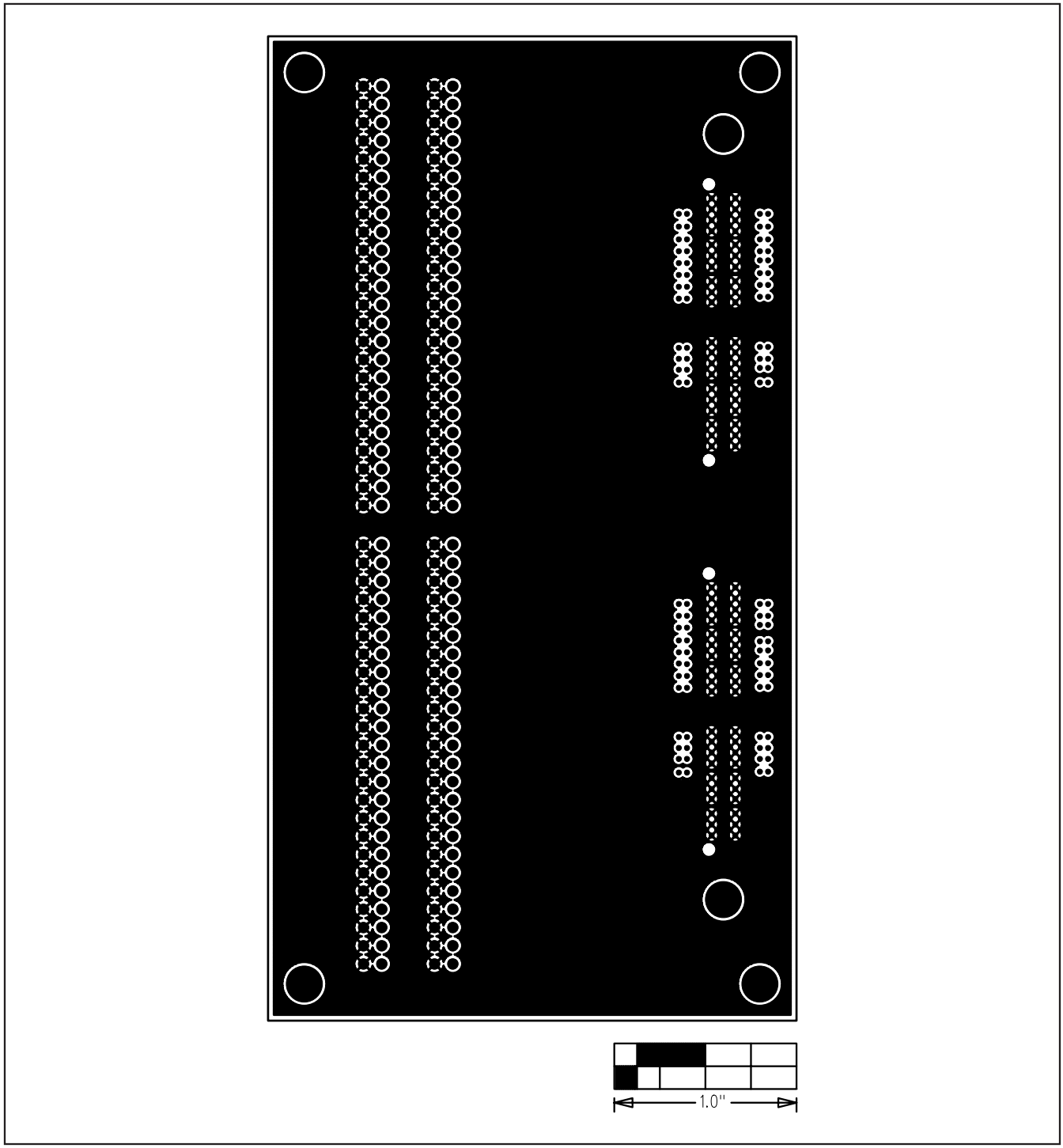

Figure 24. 12-Bit LVDS Adapter Board Layout (Inner Layer 6)—Ground Plane

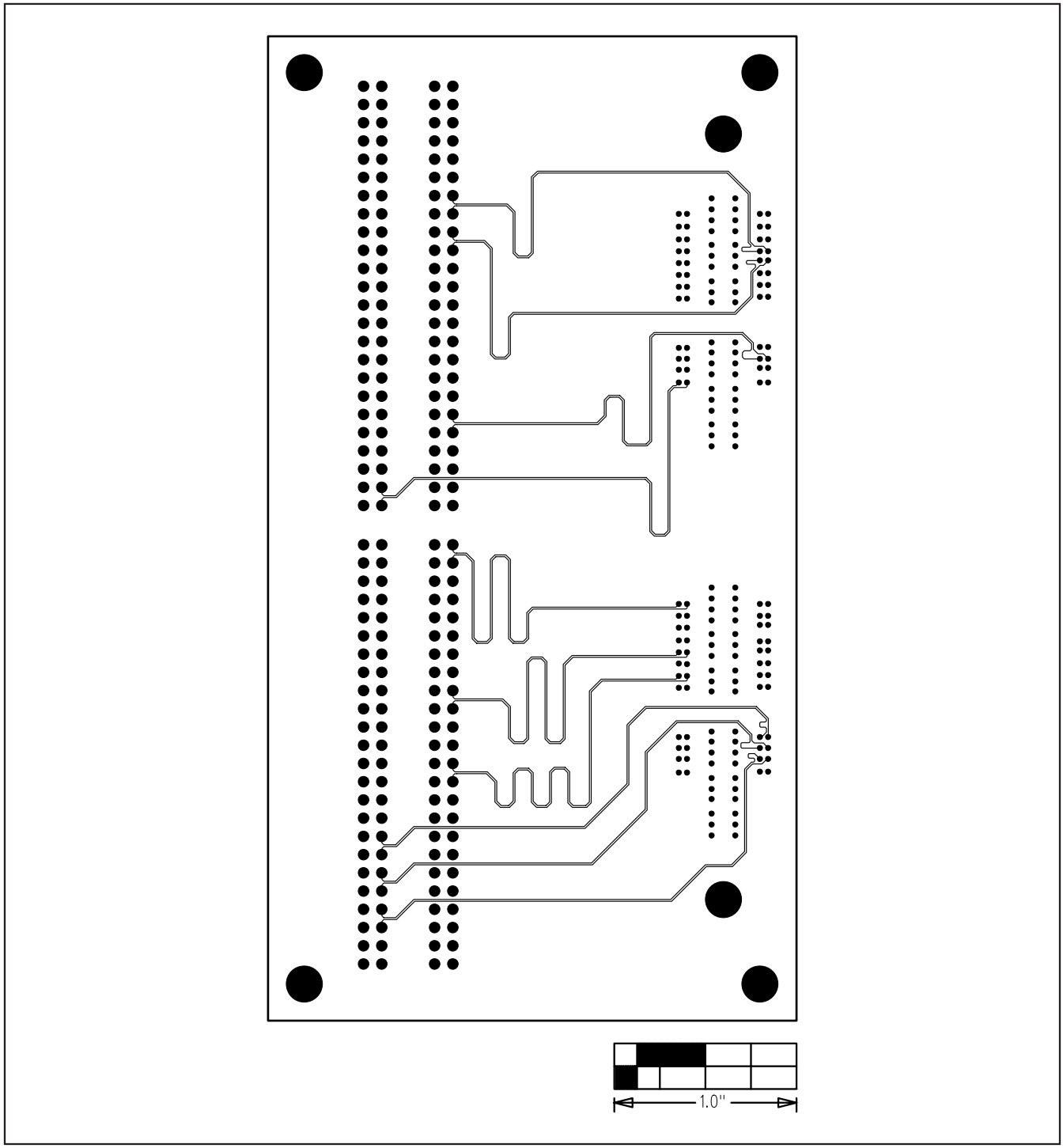

Figure 25. 12-Bit LVDS Adapter Board Layout (Inner Layer 7)—Signals

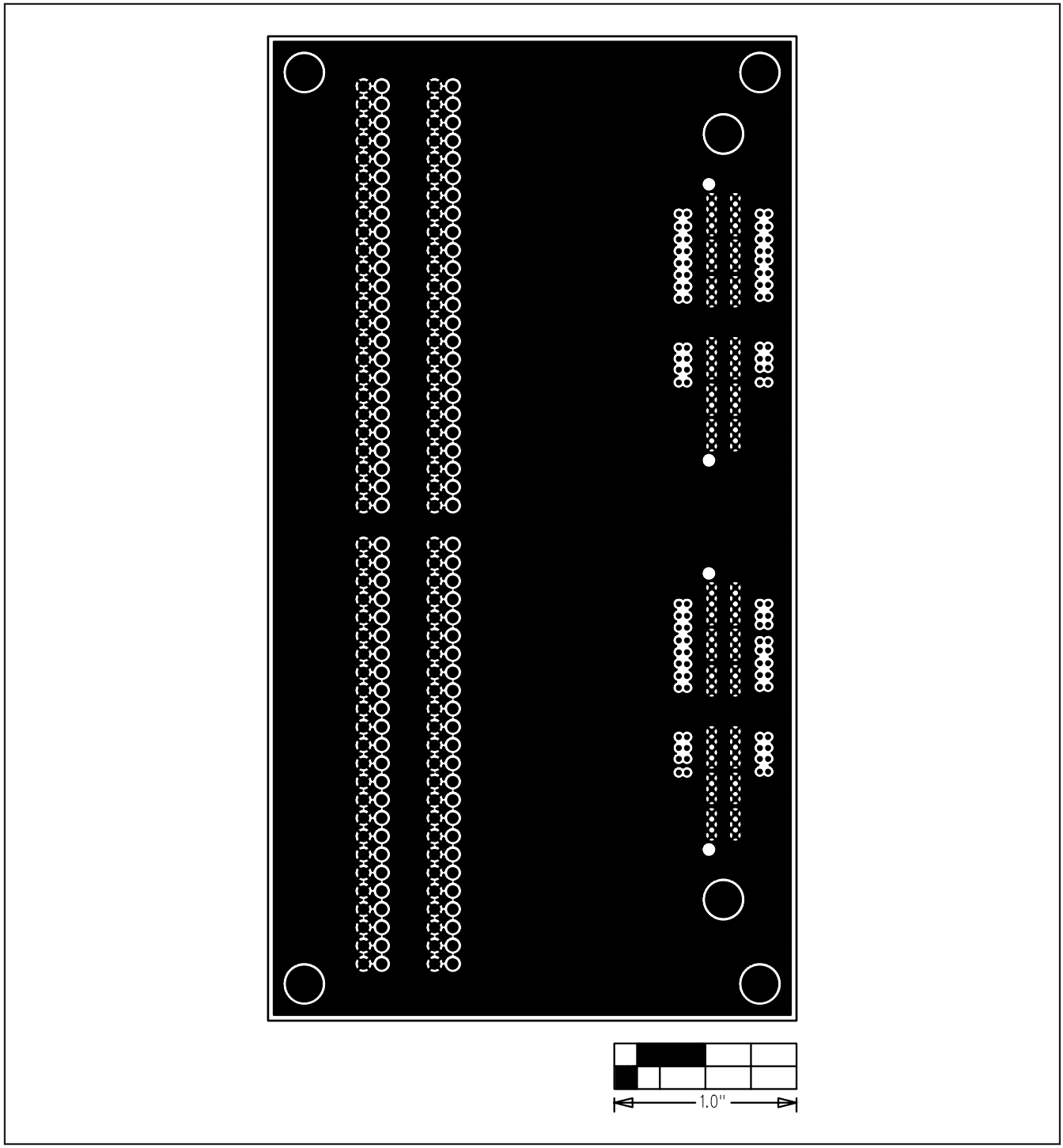

Figure 26. 12-Bit LVDS Adapter Board Layout (Inner Layer 8)—Ground Plane

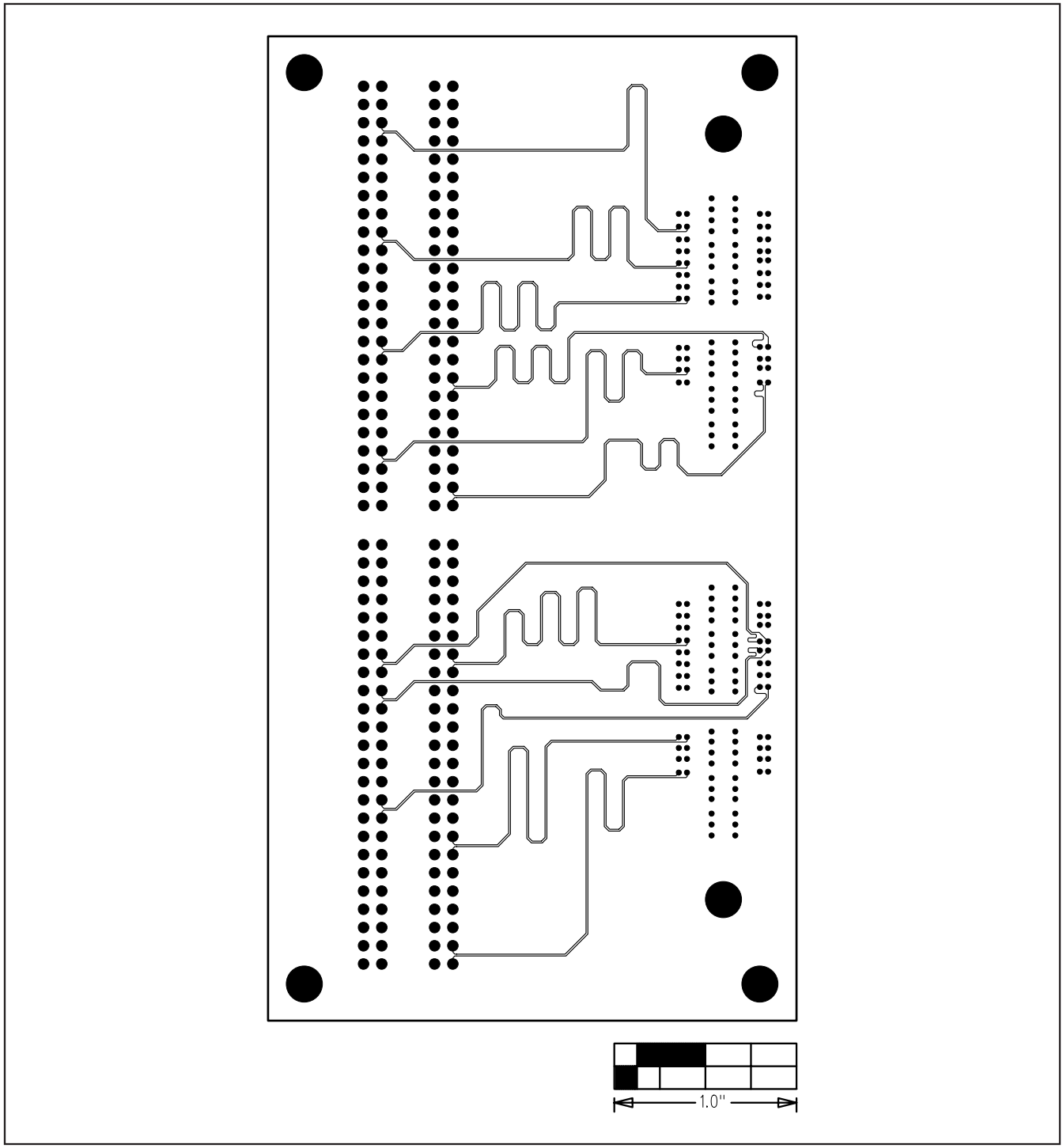

Figure 27. 12-Bit LVDS Adapter Board Layout (Inner Layer 9)—Signals

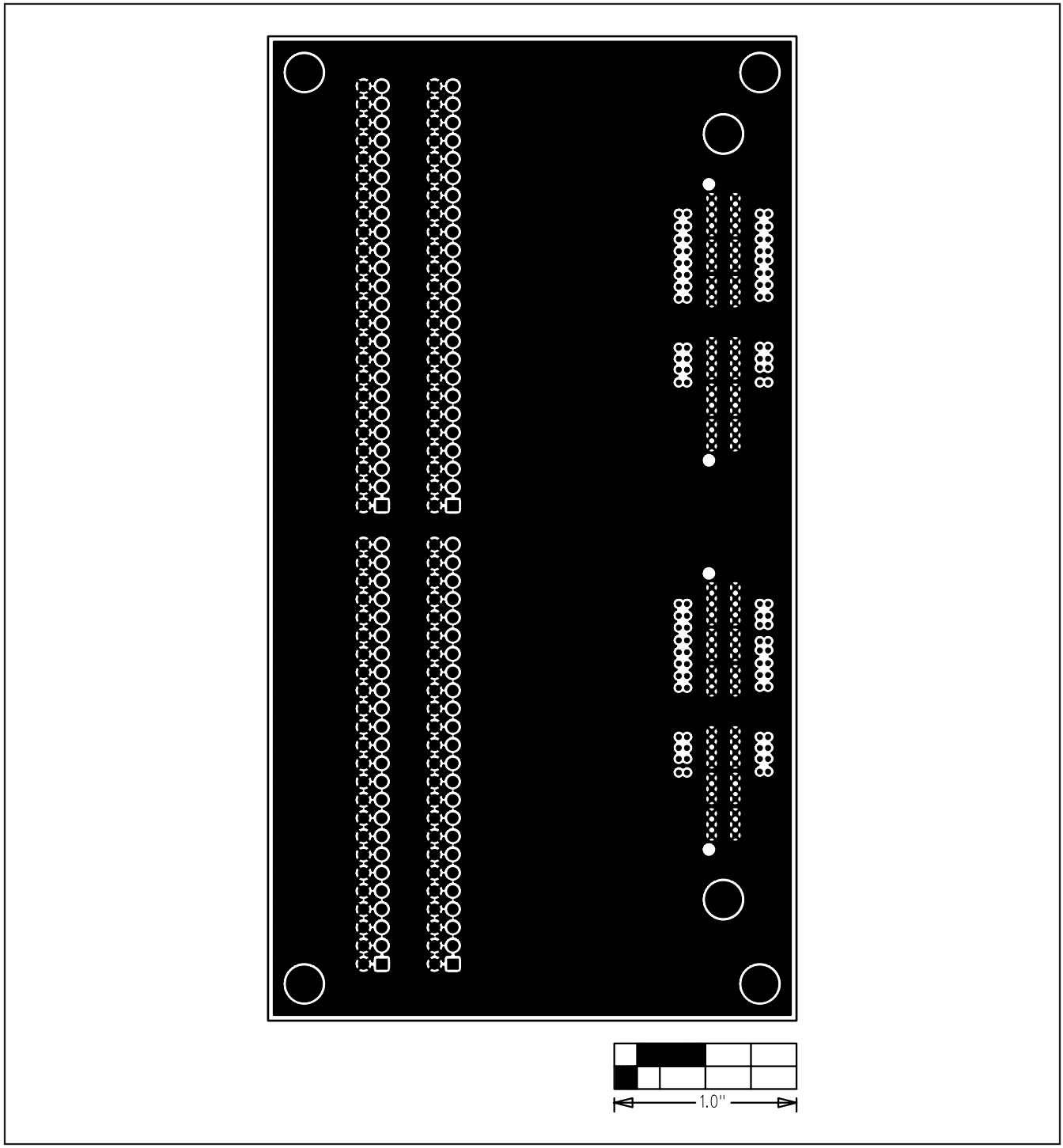

Figure 28. 12-Bit LVDS Adapter Board Layout—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	REVISION DESCRIPTION	PAGES CHANGED
0	12/06	Initial release	—
1	5/08	The EV kit board was redesigned. The same data sheet is now used for both the MAX19692 and MAX19693 EV kits.	All pages