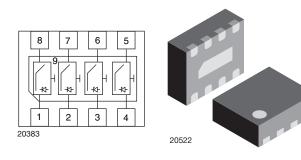
VEMI45AB-HNH

Vishay Semiconductors

4-Channel EMI-Filter with ESD-Protection



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MARKING (example only)



Dot = pin 1 marking Y = type code (see table below) XX = date code

FEATURES

- Ultra compact LLP1713-9L package
- · Low package profile of 0.6 mm
- 4-channel EMI-filter
- · Low leakage current
- Line resistance $R_S = 100 \Omega$
- Typical cut off frequency f_{3dB} = 130 MHz
- ESD-protection acc. IEC 61000-4-2 ± 18 kV contact discharge
 - ± 25 kV air discharge
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

ORDERING INFORMATION					
DEVICE NAME ORDERING CODE		TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY		
VEMI45AB-HNH	VEMI45AB-HNH-GS08	3000	15 000		

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VEMI45AB-HNH	LLP1713-9L	D	3.7 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT	
Peak pulse current	All I/O pin to pin 9; acc. IEC 61000-4-5; $t_p = 8/20 \ \mu$ s; single shot	I _{PPM}	4	А	
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V _{ESD}	± 18	kV	
	Air discharge acc. IEC6 1000-4-2; 10 pulses	VESD	± 25	ΝV	
Operating temperature	Junction temperature	TJ	- 40 to + 125	°C	
Storage temperature		T _{STG}	- 55 to + 150	°C	



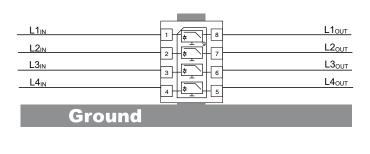


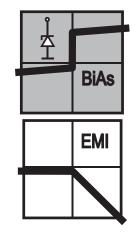


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APPLICATION NOTE

With the VEMI45AB-HNH 4 different signal or data lines can be filtered and clamped to ground. Due to the different clamping levels in forward and reverse direction the clamping behaviour is <u>Bi</u>directional and <u>Asymmetric</u> (BiAs).





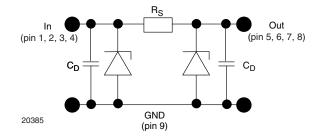
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The 4 independent EMI-filter are placed between

pin 1 and pin 8, pin 2 and pin 7, pin 3 and pin 6 and pin 4 and pin 5.

They all are connected to a common ground pin 9 on the backside of the package.

The circuit diagram of one EMI-filter-channel shows two identical Z-diodes at the input to ground and the output to ground. These Z-diodes are characterized by the breakthrough voltage level (V_{BR}) and the diode capacitance (C_D). Below the breakthrough voltage level the Z-diodes can be considered as capacitors. Together with these capacitors and the line resistance R_S between input and output the device works as a low pass filter. Low frequency signals (f < f_{3dB}) pass the filter while high frequency signals (f > f_{3dB}) will be shorted to ground through the diode capacitances C_D .



Each filter is symmetrical so that both ports can be used as input or output.

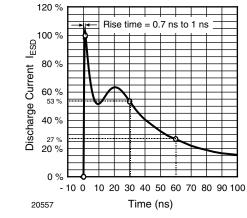
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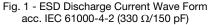


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PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of channels which can be protected	N _{channel}	-	-	4	channel
Reverse stand off voltage	Max. reverse working voltage	V _{RWM}	-	-	5	V
Reverse voltage	at I _R = 1 μA	V _R	5	-	-	V
Reverse current	at V _R = V _{RWM}	I _R	-	0.25	1	μA
Reverse break down voltage	at I _R = 1 mA	V _{BR}	6	-	-	V
Pos. clamping voltage	at I _{PP} = 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	V _{C-out}	-	-	7	V
	at $I_{PP} = I_{PPM} = 4$ A applied at the input, measured at the output; acc. IEC 61000-4-5	V _{C-out}	-	-	8	V
Neg. clamping voltage	at I _{PP} = - 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	V _{C-out}	- 1	-	-	V
	at $I_{PP} = I_{PPM} = -4$ A applied at the input, measured at the output; acc. IEC 61000-4-5	V _{C-out}	- 1.2	-	-	V
Input capacitance	at $V_R = 0 V$; f = 1 MHz	C _{IN}	-	40	45	pF
	at V _R = 2.5 V; f = 1 MHz	C _{IN}	-	24	28	pF
ESD-clamping voltage	at ± 18 kV ESD-pulse acc. IEC 61000-4-2	V _{CESD}	-	7.5	-	V
Line resistance	Measured between input and output; $I_S = 10 \text{ mA}$	R _S	90	100	110	Ω
Cut-off frequency	V_{IN} = 0 V; measured in a 50 Ω system	f _{3dB}	-	130	-	MHz

TYPICAL CHARACTERISTICS (Tamb = 25 °C, unless otherwise specified)





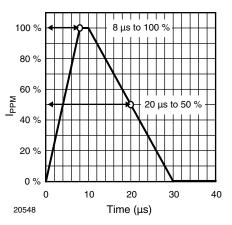
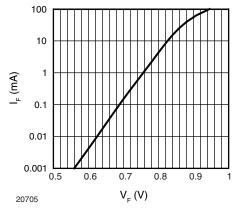


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

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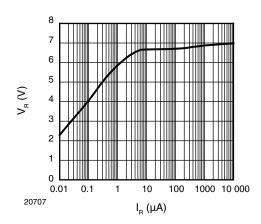


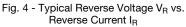
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Fig. 3 - Typical Forward Current I_F vs. Forward Voltage V_F





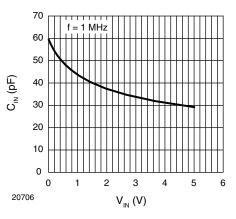


Fig. 6 - Typical Input Capacitance C_{IN} vs. Input Voltage V_{IN}

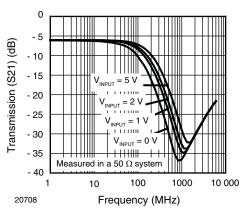


Fig. 7 - Typical Small Signal Transmission (S21) at $~Z_{O}$ = 50 Ω

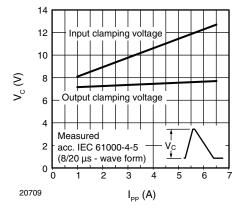


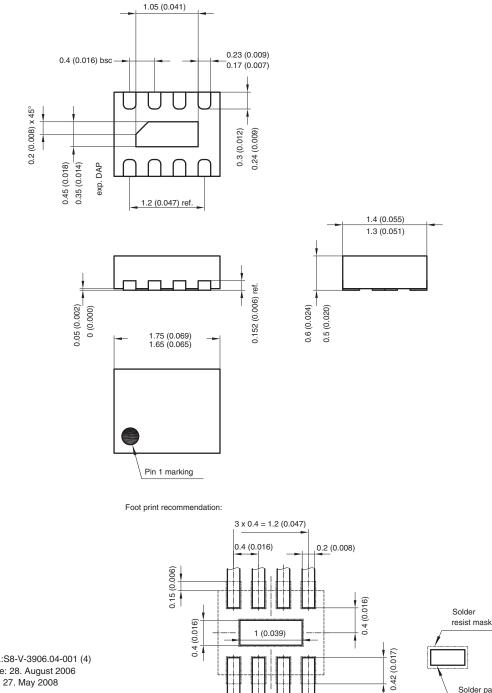
Fig. 5 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

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PACKAGE DIMENSIONS in millimeters (inches): LLP1713-9L



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Solder pad

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